A Simulation Study on the Performance Improvement of CMOS Devices Using Alternative Gate Electrode Structures

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Ich versichere hiermit an Eides statt, dass ich die vorliegende Dissertation allein und nur unter Verwendung der angegebenen Literatur verfasst habe. Die Arbeit hat bisher noch nicht zu Prüfungszwecken gedient.

Rama Subrahmanyam Komaragiri
Darmstadt, Januar 2006.

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The moments to finalize an important chapter of my life after 3 years of intensive studies on alternative gate stacks at the Institute for Semiconductor Technology have come to an end. It is the time to recognize the support I have received from many of my colleagues that throughout that period of time.

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Abstract

The success of the microelectronics industry over more then 30 years is to a large extent based on unimaginable device scaling governed by the Moore's law, which also resulted in performance improvements. The advances were mainly possible due to the unique properties of SiO_2, which is grown by thermal oxidation and poly silicon gate technologies which substituted aluminum metal gates and enabled the self aligned gate technologies. However, the aggressive scaling of Complementary Metal Oxide Semiconductor (CMOS) devices is driving SiO_2 based gate dielectrics to its physical limits as stated in the International Technology Roadmap for Semiconductors (ITRS). The scaling of device dimensions, especially the gate oxide thickness its physical limits required novel gate stack technologies, in which replacement of conventional SiO_2 with a high-K material is one of them. The usage of high-K gate materials enables the scaling of the equivalent oxide thickness (EOT) of gate dielectric into sub 1 nm regime while allowing much higher physical thickness. The feasibility of scaling EOT down to sub 1 nm results in degraded performance due to the gate oxide and non-ideal gate electrode. This work mainly discusses the performance issues of the CMOS devices and possible ways to make improvements.

When considering the biasing conditions of a CMOS device, the n^+-poly gate of a n-channel Metal Oxide Semiconductor Field Effect Transistor (NMOSFET) is biased with a positive voltage and the p^+-poly gate of a p-channel Metal Oxide Semiconductor Field Effect Transistor (PMOSFET) is biased with a negative voltage. As a result of the biasing condition, a depletion layer is formed at the gate electrode-gate oxide interface. This gate depletion is called poly gate depletion effect, results in a capacitance in series with the gate oxide capacitance. This poly gate depletion capacitance results in a decreased gate capacitance and thus results in degraded device performance. In thick oxide systems, where the gate oxide is around more than 10 nm, the gate depletion effects can be neglected as the contribution from poly gate depletion capacitance is small when compared to the gate oxide capacitance. In thin oxide systems, where the oxide thickness is less than 4 nm, the poly gate depletion effect cannot be neglected. However, degenerately doped gate electrodes can be used to suppress the poly gate depletion capacitance, by decreasing the thickness of the depletion layer formed at the gate electrode-gate oxide interface. These highly doped gate electrodes combined with thin gate oxides allow the dopants to distribute through the gate oxide and thus change the dopant distribution profile in both the gate electrode and the substrate. In ultra thin oxide systems, where the EOT is less than 2 nm, the poly gate deletion effects are unavoidable despite the gate being very highly doped. The depleted poly gate consists of parasitic charges because the ionized dopants and the parasitic charge density increases with increased doping. These parasitic gate charges act as charge centers in the gate and scatter the carries in the channel thus degrading the device performance, an effect called remote Coulomb scattering. In order to decrease the effect of remote Coulomb scattering, the parasitic gate charge density should be decreased, by reducing gate doping concentration. The reduced gate doping results in increase poly gate depletion and degrade the device performance. Thus, it is clear that the effects poly gate depletion and/or remote Coulomb scattering are unavoidable in conventionally doped gate CMOS devices.

To reduce poly gate depletion and remote Coulomb scattering, the gate depletion should be completely eliminated. Metal gates provide a possible solution to eliminate poly gate depletion completely but the integration of metal gates is difficult. In order to reduce the poly gate depletion effects, an alternative gate doping scheme, where the gate is inversely doped is proposed in this work. With inversely doped gates the poly gate depletion is eliminated selectively when the device is turned on.

The gate in conventional CMOS devices is generally of the same type as that of the source/drain, i.e., the NMOSFET has a n-gate and the PMOSFET has a p-gate. In an alternative gate doping scheme, the n-gate of the NMOSFET is replaced with a p-gate and vice versa for a PMOSFET. As a result, the gate is driven into accumulation when the device is turned on, thus retaining the gate capacitance at its maximum possible value of oxide capacitance. As the gate capacitance is retained at its maximum value, the device performance improves. The concept of alternative gate doping was verified by fabricating suitable hardware.

Through extensive simulation studies, the concept of alternate gate doping was investigated in detail. Further simulations suggested that the concept can even be implemented in silicon on insulator devices. The simulation results suggested that the device performance can be improved significantly, thus allowing the use of poly gates even in sub 100 nm regime.

Zusammenfassung

Der Erfolg der Mikroelektronik über die letzten 30 Jahre ist zu einem grossen Teil auf die Skalierung der Bauelemente zurück zu führen, die dem Moore'schen Gesetz folgt und auch die Leistungsfähigkeit erhöht hat. Die Fortschritte wurden durch die einzigartigen Eigenschaften von SiO_2 erzielt, das durch thermische Oxidation aufgewachsen wird, und zusätzlich durch die Verwendung von Polysiliziumgate-Technologien, die Aluminiumgates abgelöst und self-aligned gates möglich gemacht haben.

Die starke Skalierung von komplementären Metall-Oxid-Halbleiter (Complementary Metal Oxide Semiconductor, CMOS)-Bauelementen treibt die SiO_2-basierten Gatedielektrika an ihre physikalischen Grenzen, wie in der International Technology Roadmap for Semiconductors (ITRS) festgestellt wird. Die Skalierung der Bauelementedimensionen, inbesondere der Gateoxidedicke zu ihrer physikalischen Grenze hin erfordert neue gate stack Technologien, bei denen zum Beispiel konventionelles SiO_2 durch ein high-K Material (d.h. Material mit hoher Dielektrizitätskonstante) ersetzt wird. Die Verwendung von high-K Materialien erlaubt die Skalierung der äquivalenten Oxiddicke (equivalent oxide thickness, EOT) in den Subnanometerbereich, während die physikalische Dicke viel grösser ist. Der Einsatz von high-K-Materialien mit einer EOT im Subnanometerbereich führt allerdings zu einer verringerten Leistungsfähigkeit (performance) und der nicht-idealen Gateelektrode aus Polysislizium. Die vorliegende Arbeit behandelt diese Probleme der Leistungsminderung bei CMOS-Bauelementen und diskutiert mögliche Verbesserungsansätze.

Betrachtet man die Spannungsbedingungen eines CMOS-Baulelementes, so liegt an einem n+-Polysiliziumgate eines n-Kanal-Metall-Oxid-Halbleiter-Feldeffekttransistors (NMOSFET) eine positive Spannung an, während an einem p+-Polysiliziumgate eines p-Kanal-Metall-Oxid-Halbleiter-Feldeffekttransistors (PMOSFET) eine negative Spannung anliegt. Dadurch bildet sich eine Verarmungsschicht an der Grenzfläche von Gateelektrode und Gateoxid. Dieser Gateverarmungseffekt, der Polygate-Verarmung genannt wird, erzeugt eine Kapazität, die mit der Gateoxidkapazität in Reihe geschaltet ist. Die Polygateverarmungs-Kapazität führt zu einer verminderten Leistungsfähigkeit des Bauelements. Im Bereich dicker Oxide, wo das Gateoxid dicker als 10nm ist, können Gateverarmungseffekte vernachlässigt werden, da der Beitrag der Polygateverarmungs-Kapazität gegenüber der Gateoxidkapazität klein ist. In Dünnoxidsystemen jedoch, wo die Gateoxiddicke 4nm und kleiner ist, kann der Polygateverarmungs-Effekt nicht vernachlässigt werden. Trotzdem können entartet dotierte Gateelektroden verwendet werden, um die Polygateverarmungs-Kapazität zu unterdrücken, indem die Dicke der Verarmungsschicht an der Grenzfläche von Gateelektrode und Gateoxid verringert wird. In Verbindung mit dünnen Gateoxiden erlauben diese hochdotierten Gateelektroden die Diffusion der Dotieratome durch das Gateoxid und verändern so das Dotierprofil sowohl in der Gateelektrode als auch im Substrat. In Ultradünnoxid-Systemen mit einer EOT von weniger als 2nm sind Polygateverarmungs-Effekte unvermeidlich, auch wenn das Gate sehr hoch dotiert ist. Das verarmte Polygate enthält parasitäre Ladungen aufgrund von ionisierten Dotierstoffatomen, und die parasitäre Ladungsdichte nimmt mit steigender Dotierung zu. Die parasitären Gateladungen wirken als Ladungszentren im Gate, an denen die Ladungsträger im Kanal gestreut werden und somit die Leistungsfähigkeit des Bauelements verringern. Dieser Effekt wird "Remote Coulomb Scattering

(RCS)" genannt. Um den Effekt des RCS zu verringern, sollte die parasitäre Gateladungsdichte reduziert werden, indem die Gatedotierkonzentration verringert wird. Damit wird klar, dass einer der beiden Effekte Polygate-Verarmung und/oder RCS in konventionell dotierten Poly-Gate-CMOS-Bauelementen unvermeidbar ist.

Um sowohl Polygate-Verarmung als auch RCS zu reduzieren, sollte die Gateverarmung vollständig vermieden werden. Metall-Gates stellen einen möglichen Lösungsweg dar, aber die Integration von Metall-Gates ist schwierig. In der vorliegenden Arbeit wird ein alternatives Gatedotierungs-Schema vorgestellt, um Gateverarmungeffekte zu verringern, nämlich invers dotierte Gates. Mit invers dotierten Gates wird die Polygate-Verarmung selektiv unterdrückt, wenn das Bauelement angeschaltet ist.

Das Gate in konventionellen CMOS-Bauelementen ist im Allgemeinen vom selben Typ wie Source und Drain, d.h. ein NMOSFET hat ein n-Gate, während ein PMOSFET ein p-Gate hat. In dem alternativen Gatedotierungs-Schema wird das n-Gate des NMOSFET durch ein p-Gate ersetzt, und umgekehrt für den PMOSFET. Folglich ist das Gate in Akkumulation, wenn das Bauelement eingeschaltet wird, sodass die Gatekapazität dem maximal erreichbaren Wert der Oxidkapazität entspricht. Die Leistungsfähigkeit des Bauelements ist dementsprechend verbessert. Das Konzept der alternativen Gatedotierung wurde durch die Herstellung geeigneter Strukturen verifiziert.

Ausführliche Simulationsarbeiten dienten zur Untersuchung der alternativen Gatedotierung. Weiterführende Studien zeigten, dass dieses Konzept sich auch auf Halbleiter-auf-Isolator (Silicon on Insulator, SOI)-Bauelemente anwenden lässt. Die Simulationsergebnisse zeigten, dass die Leistungsfähigkeit der Bauelemente deutlich verbessert werden kann und Polygates somit sogar im Bereich von Gatelängen von unter 100nm benutzt werden können.

List of abbreviations

Abbreviations	Description
a.c	Alternating Current
Al_2O_3	Aluminum Oxide
BOX	Burried Oxide Layer
CDG	Conventionally Doped Gate
CMOS	Complementary Metal Oxide Semiconductor Field Effect Transistor
C-V	Capacitance Voltage Characteristics
d.c	Direct Current
DIBL	Drain Induced Barrier Lowering
DRAM	Dynamic Random Access Memory
DST	Depleted Substrate Transistor
EOT	Equivalent Oxide Thickness
FD SOI	Fully Depleted SOI
GCA	Gradual Channel Approximation
HfO_2	Hafnium Oxide
High-K	High dielectric constant insulating material
HP	High Performance
IDG	Inversely Doped Gate
ITRS	International Technology Roadmap for Semiconductors
I-V	Current Voltage characteristics
LDD	Lightly Diffused Drain
LOCOS	LOCal Oxidation of Silicon
LSP	Low Standby Power
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOSC	P-type substrate MOSC
NMOSFET	N-channel MOSFET
PD SOI	Partially Depleted SOI
PGD	Poly Gate Depletion
PGDC	Poly Gate Depletion Capacitance
PMOS	P-type substrate MOS
PMOSFET	P-channel MOSFET
Pr_2O_3	Praseodymium oxide
RCS	Remote Coulomb Scattering
RF	Radio Frequency

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Abbreviations	Description
SiO_2	Silicon dioxide
SOI	Silicon On Insulator
STI	Shallow Trench Isolation
ULSI	Ultra Large Scale Integtation
VLSI	Very Large Scale Integration
ZrO_2	Zirconium Oxide

List of symbols

Symbol	Unit	Description
χ	eV	Energy difference between vacuum level and conduction band edge in semiconductor
$\chi^{'}$	eV	Energy difference between vacuum level and conduction band edge in semiconductor
χ_i	eV	Difference between vacuum level and conduction level in insulator
δ		Linearized charge dependency constant
ΔL	cm	Reduction in channel length
ΔV_T	V	Threshold voltage shift
γ_M		Position factor of mobile ions
κ		CMOS device scaling factor
μ_l	cm^2/Vs	Mobility due to acoustic phonon interaction
μ_{n0}	cm^2/Vs	Bulk mobility of electrons
μ_{p0}	cm^2/Vs	Bulk mobility of hole
μ_{RCS}	cm^2/Vs	Mobility due to remote Coulomb scattering
μ_i	cm^2/Vs	Mobility component due to impurity scattering
μ_n	cm^2/Vs	Electron mobility
μ_p	cm^2/Vs	Hole mobility
ω	radian	Built-in potential in the p-type semiconductor substrate
ϕ_{bi}	V	Built-in potential between source/drain to substrate
ϕ_{MS}	V	Work-function difference between gate and substrate
ϕ_{pd}	V	Potential drop across poly gate depletion region
ϕ_{Sub}	V	Work-function of substrate
ϕ_f	V	Fermi potential
ϕ_G	V	Work-function of gate
ϕ_M	V	Metal work function
$\phi^{'}_M$	V	Potential difference between vacuum level and conduction band edge in metal
ϕ_n	V	Potential in n-type region
ϕ_p	V	Potential drop across a p-type bulk
ϕ_p	V	Potential in p-type region
Φ_S	V	Potential difference between vacuum level and fermi level in semiconductor
ϕ_s	V	Surface potential

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Symbol	Unit	Description
ρ_s	C/cm^2	Surface charge density
τ	s^{-1}	Mean free time between collisions
θ		Mobility reduction factor
ε	F/m	Dielectric constant
ε_K		Relative dielectric constant of high-k material
ε_{ox}		Relative dielectric constant of silicon dioxide
ε_{si}		Relative dielectric constant of silicon
ε_0	F/m	Dielectric permittivity of free space
ε_r		Relative dielectric constant
$\vec{E_n}$	V/cm	Electric field due to electrons
$\vec{E_p}$	V/cm	Electric field due to holes
$\vec{J_n}$	A/cm^2	Electron current density
$\vec{J_p}$	A/cm^2	Hole current density
Area	cm^2	Area
B	Bulk	
C$_{acc}$	F/cm^2	Accumulation capacitance
C$_{depl}$	F/cm^2	Depletion capacitance
C$_{Dsub}$	F/cm^2	Drain to substrate capacitance
C$_{GD}$	F/cm^2	Gate to drain capacitance
C$_{GS}$	F/cm^2	Gate to source capacitance
C$_{Gsub}$	F/cm^2	Gate to substrate capacitance
C$_{inv}$	F/cm^2	Inversion capacitance
C$_{ov}$	F/cm^2	Overlap capacitance of drain/source with the gate
C$_{ox}$	F/cm^2	Gate oxide capacitance
C$_{pd}$	F/cm^2	Poly gate depletion capacitance
C$_{si}$	F/cm^2	Silicon film capacitance
C$_{Ssub}$	F/cm^2	Source to substrate capacitance
C$_G$	F/cm^2	Gate capacitance
C$_K$	F/cm^2	Capacitance due to high-K material
D	Drain	
D$_n$	cm^{2}s^{-1}	Electron diffusion coefficient
D$_p$	cm^{2}s^{-1}	Hole diffusion coefficient
E$_{Fm}$	eV	Fermi level of the metal
E$_{Fs}$	eV	Fermi level in the semiconductor
E$_{ibulk}$	eV	Intrinsic Fermi level in bulk silicon
E$_{isurface}$	eV	Intrinsic Fermi level at the oxide-substrate interface of silicon
E$_0$	eV	Vacuum level
E$_C$	eV	Conduction band level in the semiconductor
E$_i$	eV	Intrinsic Fermi level in the semiconductor
E$_V$	eV	Valance band level in the semiconductor
f$_T$	Hz	Cut-off frequency
G	Gate electrode	
g$_{msat}$	Ω^{-1}	Saturation transconductance
g$_d$	Ω^{-1}	Drain conductance

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Symbol	Unit	Description
g_m	Ω^{-1}	Transconductance
I_{DS}	A	Drain current
I_{DSat}	A	Saturation drain current
k	J/K	Boltzmann constant
L	cm	Channel length
$L^{'}$	cm	Reduced channel length between source and drain
m$*$	kg	Effective mass
n		Body coefficient
n^+		Highly doped n-type silicon
n_{bulk}		Body effect coefficent of bulk CMOS devices
n_{FDSOI}		Body effect coefficent of FDSOI CMOS devices
n_{PDSOI}		Body effect coefficent of PDSOI CMOS devices
N_A	cm^{-3}	Acceptor atoms concentration
N_A^+	cm^{-3}	Ionized acceptor atom concentration
N_D	cm^{-3}	Donor atoms concentration
N_D^+	cm^{-3}	Ionized donar atom concentration
n_i	cm^{-3}	Intrinsic carrier concentration
n_s	cm^{-3}	Surface electron concentration
n	cm^{-3}	Electron concentration
p	cm^{-3}	Hole concentration
p_{bulk}	cm^{-3}	Bulk hole concentration
p_s	cm^{-3}	Surface hole concentration
q	C	Elementary charge
Q_B	C/cm^2	Charge in the bulk silicon
Q_{B0}	C/cm^2	Charge in the bulk silicon in thermal equilibrium
Q_{Bmax}	C/cm^2	Maximum charge in the bulk silicon
Q_G	C/cm^2	Charge on the gate
Q_{G0}	C/cm^2	Charge on the gate silicon in thermal equilibrium
Q_{inv}	C/cm^2	inversion charge in the channel
Q_d	C/cm^2	Charge in the depletion region
Q_G	C/cm^2	Gate charge
r_j	cm	Junction depth
S	mV/decade	Subthreshold slope
S	Source	
T	K	Absolute Temperature
t_{ox}	cm	Gate oxide thickness
t_{si}	cm	Thickness of silicon film
t_K	cm	Thickness of high-K material
U_n	$cm^{-3}s^{-1}$	Electron recombination component
U_p	$cm^{-3}s^{-1}$	Hole recombination component
V_{DS}	V	Drain to source voltage
v_{ds}	V	A.C bias of the drain to source
V_{Dsat}	V	Saturation drain voltage
V_{FB}	V	Flatband voltage
V_{GS}	V	Gate to source voltage

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Symbol	Unit	Description
v_{gs}	V	A.C bias of the gate to source
V_{ox}	V	Voltage drop across the oxide
V_{th} $(= \frac{kT}{q})$	V	Thermal equivalent voltage
V_{Tn}	V	Threshold voltage of NMOSFET
V_{Tp}	V	Threshold voltage of PMOSFET
V_B	V	Bulk voltage
V_D	V	Drain voltage
V_G	V	Gate voltage
V_S	V	Source voltage
V_T	V	Threshold voltage
W	cm	Channel width
x_{d0}	cm	Width of depleted charge region in thermal equilibrium
x_{dmax}	cm	Maximum depletion region width
x_d	cm	Depletion region width

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1 Introduction

The invention of the bipolar junction transistor by W. Shockley, J. Bardeen and W.H. Brattain in 1947 was a big step in the field of semiconductor devices. In 1958 J. Kilby demonstrated the concept of integrated circuits at Texas Instruments. This was the result of their combined efforts, which enabled the integration of semiconductor devices on a single chip. The principal of the surface field effect transistor which was proposed in early 1930's by Lilienfeld and Heil was experimentally realized by D. Kahng and M.M. Attala in 1960, resulting in the first operational Metal Oxide Field Effect Transistor (MOSFET). The concept of the integration of many semiconductor devices on a single chip, mainly with MOSFETs, provided the basis for the evolution of the microelectronics industry.

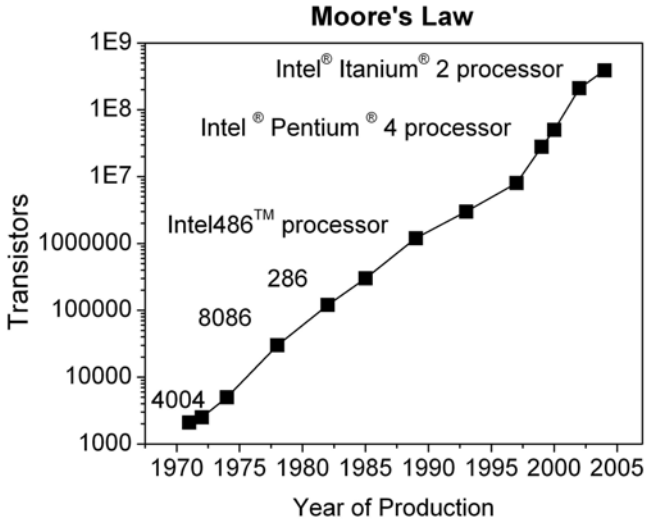

Fig. 1.1: Moore's law illustrating the exponential growth: doubling of transistors every eighteen months.

The Moore's law [1], which states the exponential increment of devices on a chip with time, is

shown in fig. 1.1 [2]. Semiconductor technology has largely advanced and MOSFETs have become by far the most important electronic device for Very Large Scale Integration (VLSI) and Ultra Large Scale Integration (ULSI) technologies.

The minimum device lateral dimension since the first demonstration of integrated circuits has been reduced from $\sim$10 μm in the 1960's to sub μm features in the 1990's. This reduction in the device dimensions resulted in huge improvements in performance and the size and weight of electronic applications were drastically reduced. Thus semiconductor devices were solely responsible for the information technology revolution in this modern era, and the MOSFET became the work horse of information technology. In order to achieve even better performance and to pack more transistors on a chip and to increase the functionality, the research is currently is being conducted towards the integration of sub 100 nm Complementary Metal Oxide Semiconductor (CMOS) Field Effect Transistors. The introduction of alternative gate stack structures with a high dielectric constant (ε_K) gate insulator and with alternative gate electrode structures is part of this work.

1.1 Modern CMOS Devices

In the 1970's scaling of the device dimensions (channel length and width, oxide thickness and junction depth) was introduced to increase the device density and to reduce the transistor costs. In the constant voltage scaling approach, the oxide voltage is kept constant whereas the oxide thickness and device dimensions are reduced which degraded the oxide integrity due to an increasing amount of oxide fields. As a result, reliability became an important issue in modern CMOS devices. The change from aluminum gate electrodes to poly silicon gates resulted in improvements in reliability and later enabled dual work function gate electrodes to optimize CMOS performance.

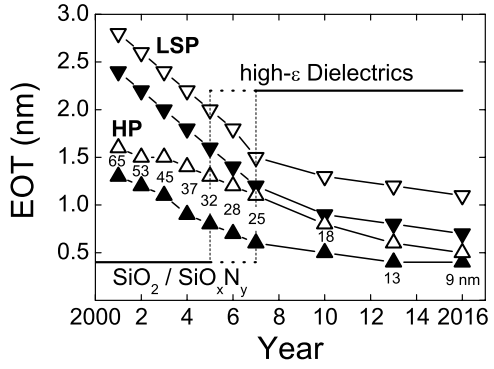

Fig. 1.2: Equivalent Oxide Thickness (EOT) versus year of introduction for both high performance and low standby power technologies. The maximum EOT (filled symbols) and minimum EOT (filled symbols) is shown for each technology generation.

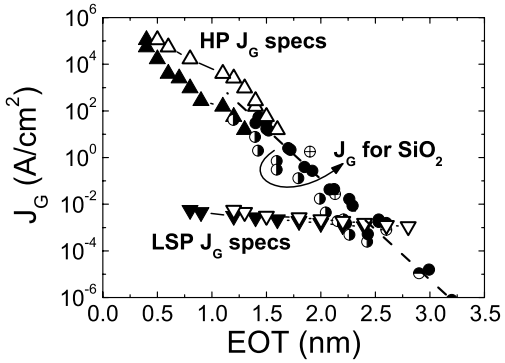

Fig. 1.3: Gate leakage current specifications versus EOT for high performance and low standby power applications. The maximum EOT (open symbols) and minimum EOT (open symbols) is shown for each technological generation. Circles indicate the experimental data for SiO_2.

The scaling requirements for future CMOS technologies is generally guided by the International Technology Roadmap for Semiconductors (ITRS) [3], where the introduction of alternative gate di-

electrics is predicted for 2005 to 2007 depending on the technology application as shown in fig. 1.2 and fig. 1.3[4]. For high performance (HP) technologies, dielectric scaling is more aggressive and will reach the sub 1 nm regime in the near future. On the other hand the leakage current requirements are more relaxed and the introduction of high-K dielectrics is not expected in HP technologies before 2007. Due to the stringent leakage requirements for low standby power (LSP) devices, the leakage current specifications cannot be met with conventional gate dielectrics in the sub 1.5 nm Equivalent Oxide Thickness (*EOT*) regime. Therefore, it is more likely that high-K dielectrics are first introduced into LSP technologies. Apart from the high performance devices and low standby power devices, aggressive scaling of devices increases the RF performance of the CMOS devices. While scaling the device dimensions the equivalent oxide thickness is scaled more aggressively and will reach sub 1 nm in near the future as shown in fig. 1.4.

The presence of different parasitic capacitances and parasitic resistances make the conventional CMOS devices to introduce more leakages. The parasitics can be reduced to a certain extent by using Silicon On Insulator (SOI) device technologies. As a result a better performance is achieved. Using novel concepts which vary from the conventional CMOS devices, the microelectronics industry managed to continuously decrease the feature size and increase the device density per chip and is expected to follow the same trends as shown in fig. 1.1.

By utilizing the scaling schemes, it is feasible to scale down the devices to the physical limits. An increase in the number of devices per given area means more complex applications can be realized in smaller dimensions and less power consumption means that the devices are portable thus making the computing *ubiquitous*.

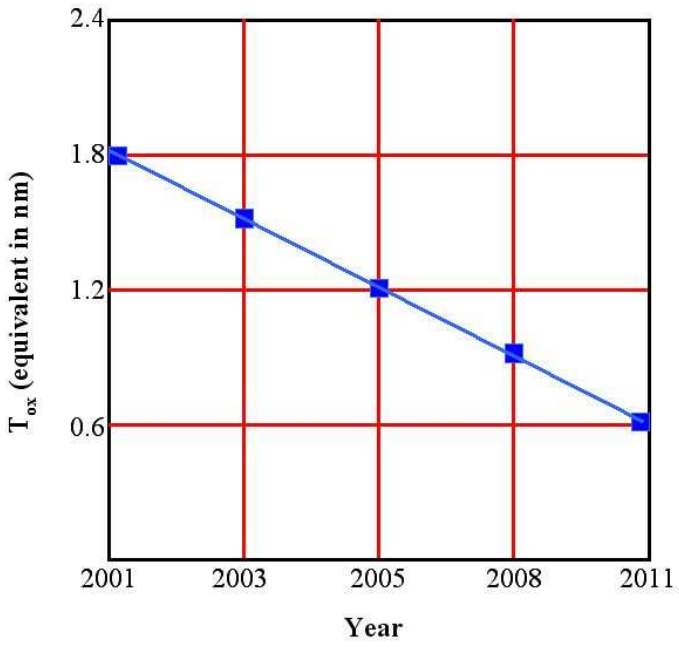

Fig. 1.4: Scaling of Equivalent Oxide Thickness as a function of time. EOT will be 1 nm around 2008.

However, the continuous scaling of devices resulted in various effects and in particular, the reduction of EOT in CMOS technologies enhanced the poly gate depletion effect [5] and gate leakage currents [6]. As a result, the performance of the devices started degrading with decreasing EOT.

The poly gate depletion effect becomes more severe in down scaling the EOT of CMOS devices as the gate oxide thickness can no longer be scaled down. Thus it became majorly important to find a solution to improve the gate stack in CMOS devices, which is the target goal of this research.

1.2 Alternative Gate Structures for Future CMOS Technologies

The primary aim of introducing alternative gate structures in place of conventional gate structures is to increase the gate capacitance and to reduce the leakage currents, which will result in improved device performance. The main factors which determine the leakage current through an insulator are the band gap, barrier height and the physical thickness of the oxide layer. To obtain low leakage currents, a larger band gap combined with a significantly higher dielectric constant compared to that of SiO_2 and barrier heights of 1.5 eV or higher are required in high-K dielectrics. The potential high-K gate dielectric materials are Al_2O_3, ZrO_2, HfO_2 and Pr_2O_3. The successful replacement of gate dielectric with a high-K material results in low leakage currents and will allow the EOT to be scaled down into sub 1 nm regime in the near future.

In order to suppress the gate depletion effects, alternative gate electrode structures are being considered. These structures usually contain metal gates. However, the metal gates are difficult to integrate.

The poly gate depletion effects can be suppressed in a very effective manner by changing the poly gate doping type in the CMOS devices. This work primarily focusses on **alternatively doped gate architectures** where the gates are inversely doped and a study on their performance relative to the conventionally doped poly gate architectures [7].

This report provides a brief overview of conventional CMOS devices in chapter 2, *The MOSFET*. The fundamentals of MOSFET are discussed with the help of the MOS capacitor. Then the biasing of the MOS capacitor is utilized to explain the working principle of the MOSFET. Deviations from the ideal to the real MOSFET, like work function difference, non ideal gate oxide properties are discussed. The current-voltage characteristics of a MOSFET are discussed along with the a.c characteristics. The effects of scaling, namely the threshold voltage roll-off and short channel effects give an insight into the effects in modern CMOS technologies. The variation in MOSFET structure, due to the variation in the bulk of CMOS devices is discussed in chapter 3, *The SOI MOSFET*, along with its characteristics. The device fabrication and a brief introduction to the simulator accounted for in chapter 4, titled *Device Fabrications and Simulations*.

Chapter 5, *The Gate Stack*, summarizes the simulation results on the gate stack and the effects, poly gate depletion and the subsequent effects of poly gate depletion on device characteristics are discussed. The possible solutions to depletion free gate electrodes and their effect on performance are explained. The *alternative gate doping scheme* is introduced as a solution to the poly gate depletion and the principle of the alternative gate doping, achieved by inversely doped gates (IDG) is explained.

Chapter 6, *Results and Discussion* summarizes the MOSFET results based on the device performance of conventional CMOS devices and SOI CMOS devices with inversely doped gates. A comparison of the device performance with conventionally doped gate devices is performed in order to understand the improvement in device performance obtained by the alternative gate doping scheme.

2
The MOSFET

2.1 Introduction

MOSFET is an acronym for Metal Oxide Semiconductor Field Effect Transistor. The MOSFET is the work horse of modern semiconductor industry and is a four terminal device. To understand the working of MOSFET, it is essential to consider a Metal Oxide Semiconductor (MOS) capacitor. Depending upon the substrate doping, a MOS capacitor can be categorized into two types: If the substrate is p-type doped, then the resulting MOS capacitor is termed a p-type MOS capacitor, or simply, PMOS capacitor. Similarly, if the substrate is n-type doped, then the MOS capacitor is an NMOS capacitor. The electrostatics of a MOS capacitor are used to explain the working of a MOSFET, so it is important to study the electrostatics of a MOS capacitor in detail to understand the MOSFET, which is looked at in the next section. In addition, this chapter gives an overview of the device characteristics of a MOSFET.

2.2 The MOS Capacitor

A MOS capacitor is a two terminal device with an insulator, known as a gate insulator. It is usually silicon-dioxide (SiO_2), sandwiched between gate electrode (G) and semiconductor substrate (B), also known as bulk which is shown in fig. 2.1. The gate insulator and gate electrode together are called gate stack. Generally the gate is biased while the substrate is grounded. In the following sections the electrostatics of the MOS capacitor will be discussed.

2.2.1 MOS Capacitor Electrostatics

In a MOS capacitor, the applied gate voltage influences the charge distribution in the area just below the oxide-substrate interface. Depending on the gate bias, a MOS capacitor can be biased in three different regimes namely: accumulation, depletion and inversion. Now we will briefly discuss, with the help of energy band diagrams, how different biasing conditions will effect the MOS capacitor [8], [9], [10].

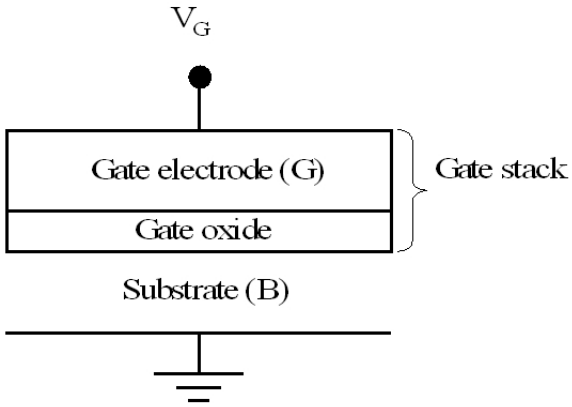

Fig. 2.1: Schematic diagram of a MOS capacitor.

In the following analysis, unless otherwise specified, the substrate is of p-type. For the first pass assume an ideal MOS capacitor with a perfect gate oxide, without any charges in the oxide and the gate oxide-substrate is free from interface states. The other important assumption is that, there is no difference in the work function of the metal gate and the bulk semiconductor, which means that the fermi level of the gate electrode and the fermi level of the substrate are aligned at the same level when no external bias is applied.

2.2.2 MOS Capacitor in Thermal Equilibrium With Zero Applied Bias

In an ideal MOS capacitor with the specifications mentioned above, the potential in the silicon substrate is given as:

$$\phi_f = -V_{th} \ln \left(\frac{N_A}{n_i} \right) \tag{2.1}$$

where ϕ_f is the fermi potential, V_{th} is the thermal voltage given as kT/q with k being the Boltzmann's constant, T is absolute temperature, q is elementary charge, N_A is the acceptor doping concentration in the substrate and n_i is intrinsic carrier concentration. This potential, ϕ_f is also equivalent to the potential difference or energy difference between the intrinsic fermi level, E_i and the quasi fermi level E_{Fs} as shown in fig. 2.2.

When the gate electrode and the substrate are connected together in thermal equilibrium, the aligned fermi levels in the gate electrode and substrate means that there is no internal potential drop across the structure. This condition is called *flat band condition*, as the energy bands are flat throughout the structure. The corresponding voltage is called flat band voltage V_{FB} and for an ideal MOS capacitor, $V_{FB} = 0$. The energy band diagram of a PMOS capacitor in thermal equilibrium with zero applied bias is shown in fig. 2.2 with E_0 being the vacuum level, which is the minimum amount of energy an electron must possess to completely free itself from the material. E_{Fm} is the metal fermi level and the difference between the vacuum level and the fermi level of the metal, is also known as the metal work function $q\phi_M$. χ is the energy difference between the vacuum level and the minimum of conduction band edge (E_C) in the semiconductor, E_i is the intrinsic fermi level located in the middle of the band gap at absolute zero, E_{Fs} is the fermi level of the semi conductor, E_V is the maximum of the valance band energy level and $q\Phi_s$ is the energy difference between the vacuum level and the fermi level the of the semiconductor. χ_i is the energy difference between the vacuum level and the minimum of conduction band edge in the insulator, while t_{ox} is the thickness of the gate oxide.

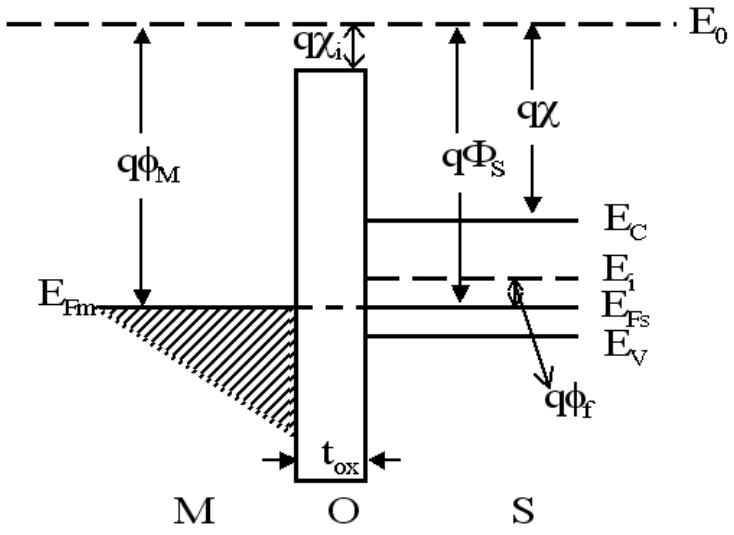

Fig. 2.2: Energy band diagram of an ideal PMOS capacitor in thermal equilibrium illustrating the flat band condition.

2.2.3 MOS Capacitor Under Applied Bias

In considering the effect of gate bias on the MOS capacitor, the best point to start the analysis is when the potential drop across the MOS capacitor is zero, i.e, the flat band condition. As there is no internal potential drop across the structure, the resultant charge on the gate is zero. Thus, at flat band:

$$Q_G\left(V_G = V_{FB}\right) = 0 \tag{2.2}$$

When the voltage on the gate is decreased below V_{FB}, i.e, when a negative voltage is applied on

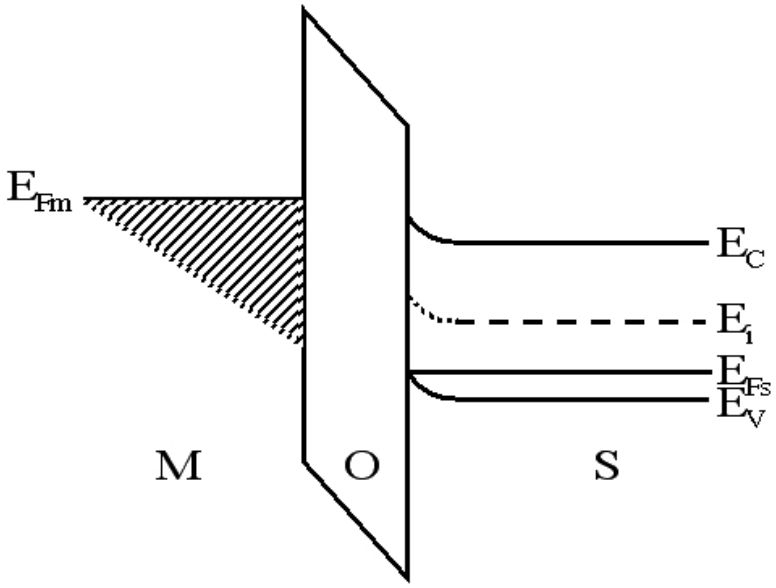

Fig. 2.3: Energy band diagram of a PMOS capacitor in accumulation, ($V_G < 0$).

the gate, the E_{Fm} relative to E_{Fs} raises. The negative bias on the gate results in the attraction

of holes in the semiconductor. As a result, the positive charge concentration in the substrate near the gate oxide-substrate interface increases. This causes a negative slope of energy bands in both the insulator and semiconductor, as shown in fig. 2.3. This particular biasing condition, where the majority carrier concentration at the oxide-silicon interface is greater than the majority carrier concentration in the bulk silicon is known as *accumulation*, for $V_G < V_{FB}$. As the net charge in the structure is zero, the charge residing on the gate should be equal and opposite to the charge in the semiconductor. In accumulation, the charge distribution in the PMOS capacitor is illustrated in fig. 2.4. In accumulation, the gate charge is given as:

$$Q_G = C_{ox}(V_G - V_{FB}) \qquad for \qquad V_G \leq V_{FB} \tag{2.3}$$

where $C_{ox}=\varepsilon_{ox}\varepsilon_0/t_{ox}$ is the gate oxide capacitance per unit area. The applied gate voltage drops across the oxide and substrate. The potential distribution in a PMOS capacitor is as illustrated in fig. 2.5. Further reduction in the gate voltage results an increased accumulation charge at the oxide-substrate interface.

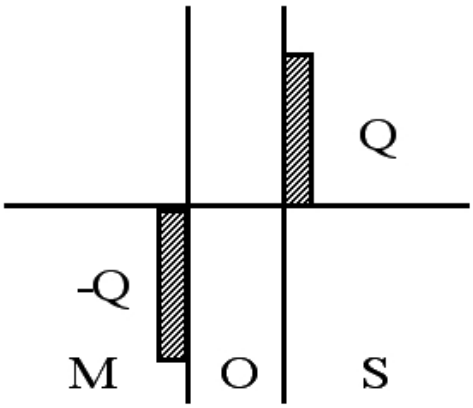

Fig. 2.4: Distribution of charges in a PMOS capacitor in accumulation ($V_G < 0$).

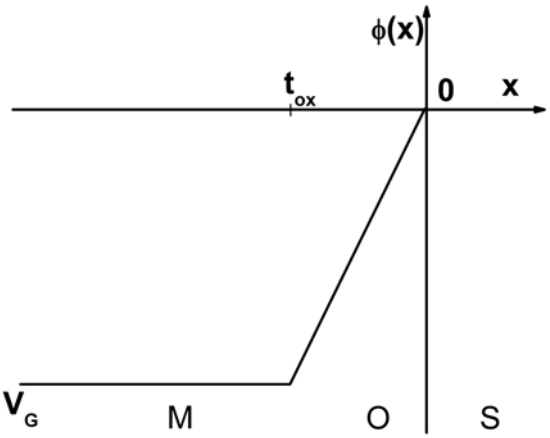

Fig. 2.5: Potential distribution across a PMOS capacitor when the gate is biased accumulation ($V_G < 0$).

When the applied gate voltage $V_G > V_{FB}$ is positive, the number of positive charges on the gate increases with increased gate bias. This positive charge attracts electrons near to the oxide-substrate interface, and, therefore, a compensating negative charge layer just beneath the gate oxide-silicon interface is formed. As a result, the hole concentration at the oxide-silicon interface decreases when compared to the hole concentration in the bulk silicon. Thus the oxide-silicon interface is depleted of holes, and the PMOS capacitor is said to be in *depletion*. As a result of reduced hole concentration at the oxide-silicon interface, the bands bend downward as shown in fig. 2.6.In depletion, only negatively ionized impurity atoms remain in close proximity to the oxide-substrate interface. This forms a depletion region at the gate electrode-gate oxide interface. The width of the depletion region $x_d(V_G)$, as a function of gate bias V_G is given as:

$$x_d(V_G) = t_{ox}\frac{\varepsilon_{si}}{\varepsilon_{ox}}\left(\sqrt{1+\frac{2C_{ox}^2\left(V_G - V_{FB}\right)}{q\varepsilon_{si}\varepsilon_0 N_A}} - 1\right) \tag{2.4}$$

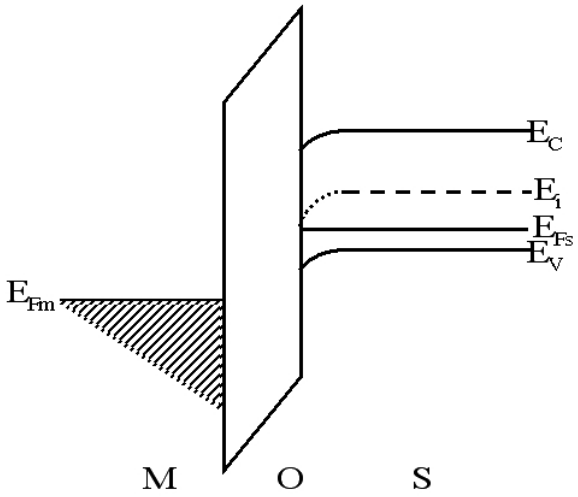

Fig. 2.6: Energy band diagram of a PMOS capacitor in depletion ($0 < V_G$).

The gate charge in the depletion is equal and opposite in sign to the bulk charge and is given as:

$$Q_G(V_G) = -Q_B = qN_A x_d(V_G) \tag{2.5}$$

In addition we define the potential drop at the oxide-substrate interface as the surface potential (ϕ_s). The surface potential is a measure of the amount of depletion charges created at the oxide-substrate interface. The surface potential, ϕ_s is given as:

$$\phi_s(V_G) = V_G - \left(\frac{qN_A x_d(V_G)}{C_{ox}}\right) \tag{2.6}$$

The applied gate voltage drops across the structure, which can be divided in to four parts, a constant voltage drop in the metal gate electrode, a linear drop across the oxide, a varying potential distribution in the depleted region, a non linear decrease in the depletion region and constant in the substrate beyond x_d. The charge and potential distributions of the MOS capacitor when in depletion are shown in fig. 2.7 and fig. 2.8 respectively.

However, when the gate voltage is further increased, the width of the depletion region x_d reaches a maximum possible value so that the number of ionized negative impurity atoms cannot compensate the positive gate voltage drop. The hole concentration at the oxide-substrate interface decreases and electron concentration gradually increases. At a particular gate voltage, the electron concentration at the oxide substrate interface is the same as the bulk hole concentration. This condition is known as *onset of inversion*. At the onset of inversion, the surface potential reaches a value, opposite and equal to the fermi potential of the substrate. Thus at the onset of inversion, the surface potential is given as:

$$\phi_s = -\phi_f \tag{2.7}$$

and the surface electron concentration n_s, at the onset of inversion is given as:

$$n_s = n_i e^{\frac{\phi_s}{V_{th}}} = n_i e^{\frac{-\phi_f}{V_{th}}} = p_{bulk} = N_A \tag{2.8}$$

$$n_s = n_i e^{\frac{E_{isurface} - E_{ibulk}}{kT}} = n_i e^{\frac{E_{Fs} - E_{ibulk}}{kT}} = p_{bulk} = N_A \tag{2.9}$$

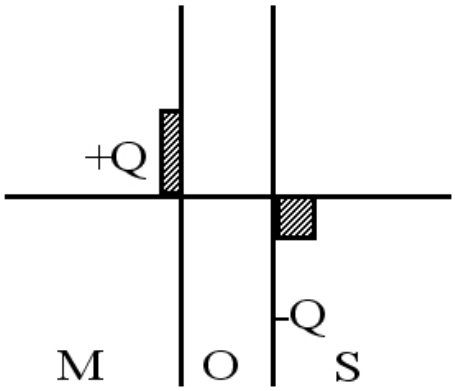

Fig. 2.7: Distribution of charges in a PMOS capacitor in depletion ($0 < V_G$).

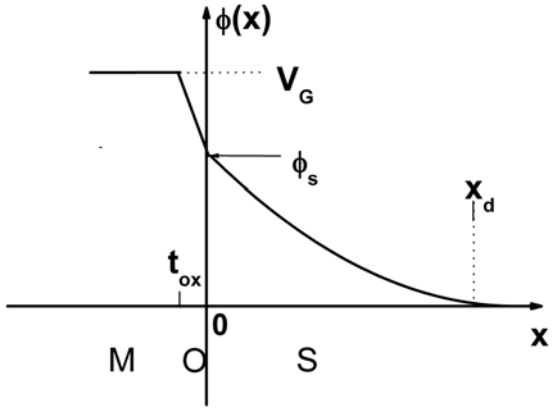

Fig. 2.8: Potential distribution in a PMOS capacitor in depletion ($0 < V_G$).

where p_{bulk} is the hole concentration in the bulk, E_{ibulk} is the intrinsic fermi level far away from the oxide-substrate, while $E_{isurface}$ is the intrinsic fermi level at the oxide-substrate interface. When the

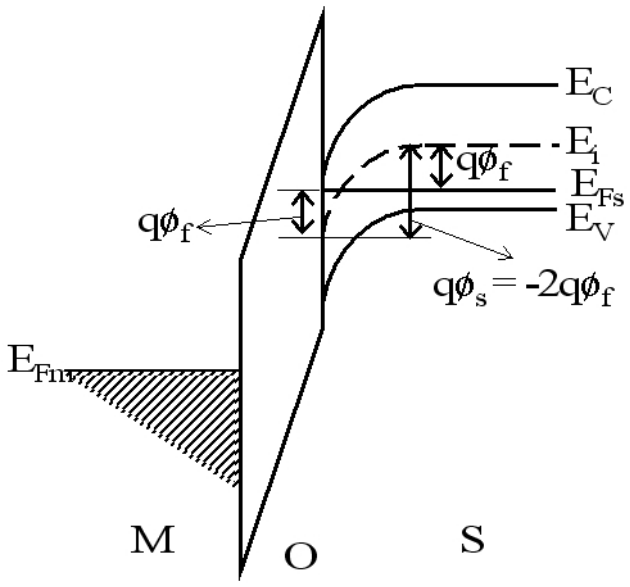

Fig. 2.9: Energy band diagram of a PMOS capacitor in inversion, ($0 < V_G$).

gate voltage is further increased beyond onset of inversion, the surface potential ϕ_s will continue to increase and eventually reaches a value of -2ϕ_f. This condition is called *inversion* and the MOS capacitor is said to be inverted as shown in the fig. 2.9. After inversion, with increasing gate bias,

the surface potential does not change much due its logarithmic dependency on the bulk doping concentration, and thus for all practical purposes, the surface potential remains pinned at -$2\phi_f$. The voltage at which $\phi_s = -2\phi_f$ occurs is known as the threshold voltage V_T of the MOSC.

In inversion, the depletion region width and the charge in the depletion region attain their maximum values, given as:

$$x_{dmax} = \sqrt{\frac{2\varepsilon_{si}\varepsilon_0(-2\phi_f)}{qN_A}} \tag{2.10}$$

and

$$Q_{Bmax} = -qN_A x_{dmax} = -\sqrt{2q\varepsilon_{si}\varepsilon_0 N_A(-2\phi_f)} \tag{2.11}$$

The gate charge can be calculated as:

$$Q_G = C_{ox}\left(V_G - V_T\right) + \frac{q\varepsilon_{si}\varepsilon_0 N_A}{C_{ox}}\left(\sqrt{1 + \frac{2C_{ox}^2\left(V_T - V_{FB}\right)}{q\varepsilon_{si}\varepsilon_0 N_A}} - 1\right) \tag{2.12}$$

The charge and potential distributions of a MOS capacitor under inversion are shown in fig. 2.10 and fig. 2.11 respectively.

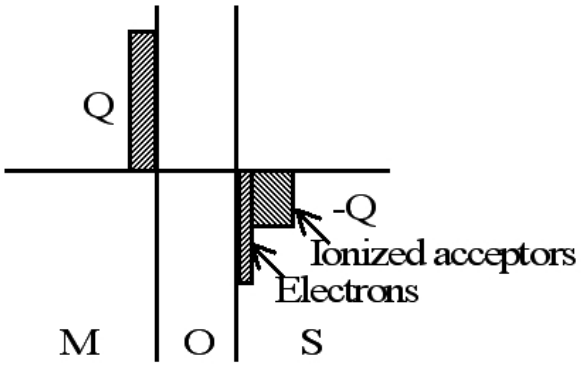

Fig. 2.10: Distribution of charges in a PMOS capacitor in inversion ($0 < V_G$).

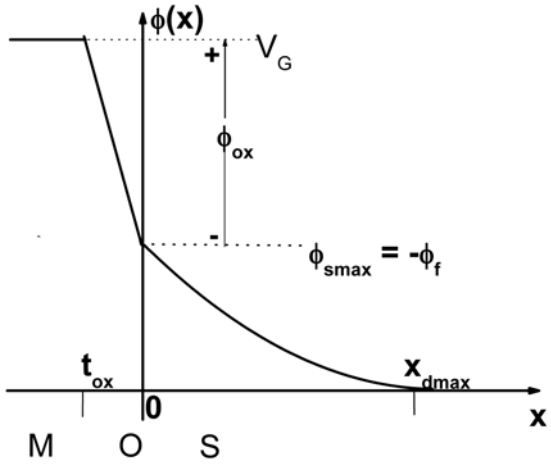

Fig. 2.11: Potential distribution in a PMOS capacitor in inversion ($0 < V_G$).

2.2.4 Threshold Voltage

The applied gate voltage, at which ϕ_s = -$2\phi_f$ occurs is defined as the *threshold voltage*, V_T of a MOS capacitor. Depending on the substrate doping type, V_{Tn} is the threshold voltage of the PMOS capacitor while V_{Tp} is the threshold voltage of a NMOS capacitor. As the voltage applied to the gate drops across the oxide and bulk, at onset of inversion, the gate voltage applied to the PMOS capacitor is given as

$$V_G = V_{Tn} = V_{FB} + V_B + \phi_{ox} = V_{FB} - 2\phi_f + \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}\varepsilon_0 N_A(-2\phi_f)} \tag{2.13}$$

Similarly for a NMOS capacitor the threshold voltage(V_{Tp}) is given as:

$$V_G = V_{Tp} = V_{FB} - 2\phi_f - \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}\varepsilon_0 N_D(2\phi_f)} \tag{2.14}$$

Table 2.1 summarizes various gate biasing conditions of both PMOS capacitor and NMOS capacitor.

	PMOS capacitor	NMOS capacitor
Accumulation	V_G<0	V_G>0
Depletion	V_T>V_G>0	V_T<V_G<0
Inversion	V_G>V_T	V_G<V_T

Table 2.1: Different biasing regions of a PMOS capacitor and NMOS capacitor.

2.3 Non Ideal MOS Capacitor

The ideal MOS capacitor discussed in section 2.2.1 is far from reality, even though the ideal structure provides a convenient way in which to understand the real MOS capacitor is easier. The real MOS capacitor deviates from the ideal MOS capacitor in various ways. The important deviations are:

- work function difference
- oxide charges
- non-ideal gate stack

2.3.1 Work Function Difference

The assumption of equal work function of the metal gate and bulk semiconductor is a simplification and very unlikely to happen in real structures. Thus, in a real MOS capacitor, there is a finite work-function difference between the metal and semiconductor which is described as:

$$q\phi_M \neq q\phi_s = q\chi + \left(E_C - E_{Fs}\right)_{FB} \tag{2.15}$$

In equilibrium, with no applied gate bias, $V_G = 0$, the alignment of metal fermi level (E_{Fm}) with semiconductor fermi level (E_{Fs}) in combination with eqn. (2.15) requires that the vacuum levels of metal and the semiconductor must be at different energy levels. As a consequence an electric field develops between the semiconductor vacuum level and the metal vacuum level. The direction of electric field depends upon the sign of the work function difference. Assuming the metal work function to be less than the semiconductor work function, the developed electric field results in the silicon vacuum level being above that of the metal vacuum level. As a result the effective surface barriers in the oxide and in the semiconductor bend downward as shown in the fig. 2.12 [8]. The bending of surface barriers results in a band bending in the silicon substrate near the oxide-silicon interface. The potential drop in the oxide and semiconductor as a result of the work function difference is given as:

$$\phi_{MS} = \phi_M - \phi_s = \phi_M^{'} - \chi^{'} - \frac{1}{q}\left(E_C - E_{Fs}\right)_{FB} \tag{2.16}$$

where $\phi_M^{'} = \phi_M - \phi_s$ and $\chi^{'} = \chi - \Phi_S$. From fig. 2.12, it is noticeable that $V_G = 0$ does not give rise to the flat band condition inside the semiconductor. To achieve the flat band condition in the

semiconductor, a negative bias, equal to the work function difference ϕ_{MS} should be applied to the gate. The flat band voltage of a PMOS capacitor is now equal to ϕ_{MS}. As a result of the work function difference, the threshold voltage of the MOS capacitor shifts by a value equal to ϕ_{MS}.

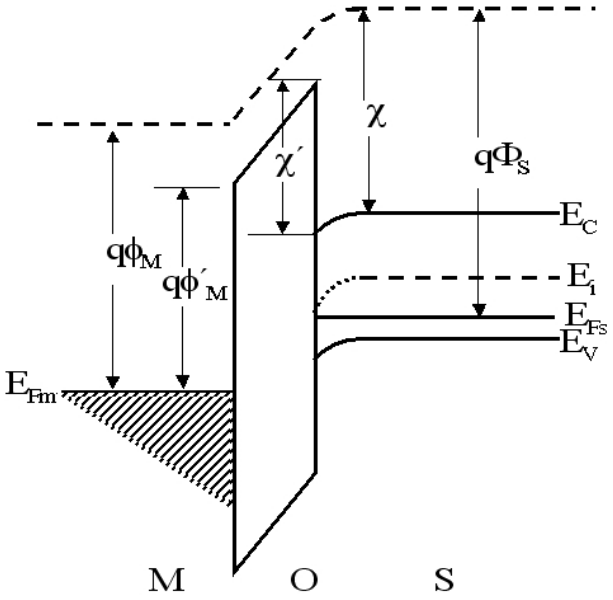

Fig. 2.12: Schematic band diagram of a PMOS capacitor in depletion with a work function difference between the gate electrode and substrate.

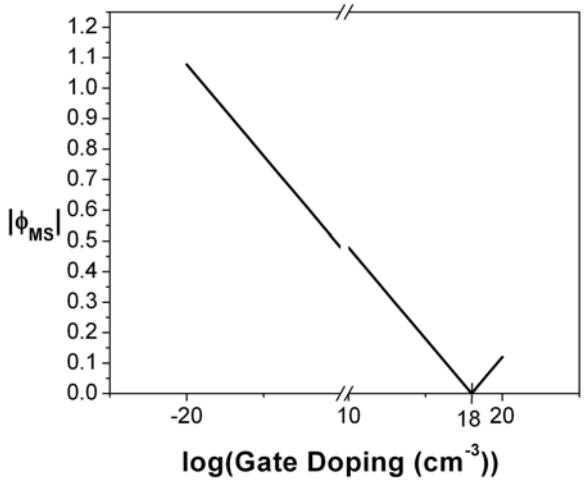

Fig. 2.13: Change in work function difference of a capacitor with a change in gate doping concentration. The reference gate doping is taken as 10^{18} phosphorus atoms cm^{-3} for a fixed substrate doping.

In modern CMOS technologies with highly doped poly silicon gate electrodes, where a dual work function approach is practiced; i.e, a PMOS capacitor has a n-type doped poly gate and a NMOS

capacitor has a p-type poly doped gate, the threshold voltage can be adjusted by varying the doping concentration of the gate. For example, if N_D is the doping concentration of the gate and N_A is doping concentration of the substrate, then the work function difference will be

$$\phi_{MS} = \phi_{Gate} - \phi_{Sub} = \frac{kT}{q} \ln \left(\frac{N_D}{N_A} \right) \tag{2.17}$$

where ϕ_{Gate} is the work function of the gate electrode and ϕ_{Sub} is the work function of the substrate. Thus by changing the gate doping, the threshold voltage of the MOS device can be varied over a wide range. Fig. 2.13 briefly summarizes the change in ϕ_{MS} of a PMOS capacitor, when the gate doping is changed from 10^{18} cm^{-3} phosphorus atoms (positive doping) to 10^{20} cm^{-3} and then to 10^{20} cm^{-3} boron atoms (negative doping).

2.3.2 Oxide Charges

The most general assumption that was made in the MOS capacitor analysis apart from zero work function difference is that the oxide is charge and defect free. In reality, some charges actually exist inside the oxide. The different types of oxide charges are illustrated in fig. 2.14. The main effect of these charges is a shift in the flat band voltage (V_{FB}) and thus effecting the threshold voltage (V_T) of the device. In the long run, these charges can cause instability to the device and are an issue of reliability. The oxide charges which mainly contribute to the device properties are

1. mobile ions
2. fixed oxide charges
3. interface traps
4. oxide trapped charges

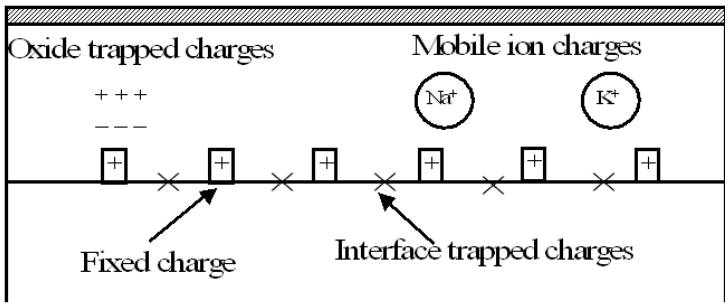

Fig. 2.14: Schematic representation of charges in gate oxide in a MOS capacitor.

The shift in threshold voltage due to oxide charges is given as:

$$\Delta V_T = (V_{TReal} - V_{Tideal})|_{\phi_s} = -\frac{Q_F}{C_{ox}} - \frac{\gamma_M Q_M}{C_{ox}} - \frac{Q_{IT}(\phi_s)}{C_{ox}} \tag{2.18}$$

where Q_F is the fixed oxide charge density, Q_M is the mobile ion charge density and Q_{IT} is the interface trapped charge density and γ_M is the position dependent factor of mobile ions. When all the mobile ions are at gate electrode-to-oxide interface, $\gamma_M \longrightarrow 0$ and when all mobile ions are at oxide-to-substrate interface $\gamma_M \longrightarrow 1$.

2.3.3 Non Ideal Gate Stack

In conventional MOS devices the dielectric constant of a gate oxide (ε_{ox}) is much smaller than the dielectric constant of the silicon substrate (ε_{Si}). If a high-K material (whose dielectric constant ε_K is greater than ε_{ox}) replaces SiO_2 as gate dielectric, due to scaling, the properties of the gate stack differ from the ideal oxide silicon stack, as discussed in section 2.8. The poly silicon gate can no longer be a perfect electrode as even degenerately doped poly silicon introduces an effect called poly silicon gate depletion or poly gate depletion. This is discussed in section 2.8.2.1.

2.3.4 C-V Characteristics

The capacitance-voltage (C-V) characteristics give information to the charge distribution and various types of charges and traps are present in the MOS capacitor structure [8], [11]. The C-V characteristics serve as a powerful diagnostic tool for identifying deviations from the ideality in both the oxide and semiconductor. The C-V characteristic curves are traced by finding the change in charge together with the change in gate bias, resulting in the differential capacitance. A small a.c signal is applied over a d.c gate bias and the d.c bias is systematically changed from accumulation through depletion to inversion. At a fixed gate bias, the change in the gate charge with respect to applied a.c bias is given as:

$$C = \frac{dq_G}{dv_G}\Big|_{V_G} \tag{2.19}$$

In accumulation, the majority carriers pileup at the oxide-semiconductor interface. The majority carriers can follow the change in gate bias and can reach equilibrium when the applied gate voltage changes very rapidly. The charge follows the applied a.c signal even for high frequencies (e.g. 1MHz). Thus the MOS capacitor in accumulation is like a parallel plate capacitor and the accumulation capacitance (C_{acc}) is given as:

$$C_{acc} = C_{ox} = \frac{\varepsilon_{ox}\varepsilon_0}{t_{ox}} \tag{2.20}$$

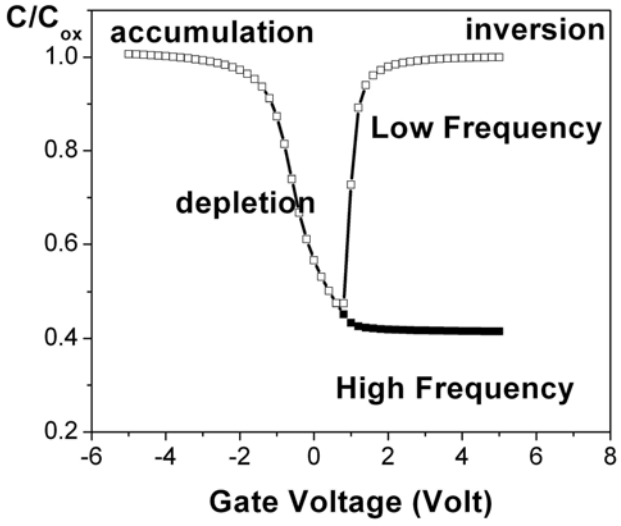

Fig. 2.15: Capacitance-voltage characteristics of a PMOS capacitor.

When the PMOS capacitor is depletion biased, a positive charge on the gate and a negative charge in the depletion region of width x_d in the semiconductor forms. When the a.c signal introduces a positive charge on the gate, the depletion layer width in the semiconductor widens instantaneously and only majority carriers are still involved in the action, i.e, the depletion width follows the applied gate voltage for high frequencies (several MHz). Thus, the situation is analogous to two parallel plate capacitors in series, the oxide capacitance (C_{ox}) and the semiconductor capacitance (C_{si}). Thus the depletion capacitance (C_{depl}) is given as:

$$C_{depl} = \frac{C_{ox}}{1 + \frac{\varepsilon_{ox} x_d}{\varepsilon_{si} t_{ox}}} \tag{2.21}$$

The depletion region width x_d changes with the gate bias in a MOS capacitor, from eqn. (2.21) the C_{depl} is a function of the depletion width x_d. The depletion width increases with an increase in gate bias according to eqn. (2.4). As a result, the depletion capacitance decreases with an increasing gate bias. When the gate is inversion biased, the minority carriers pile up at the oxide-semiconductor interface and the depletion width tends to maximize at a value x_{dmax}. The excess charge created or removed will now be a function of the frequency of the applied a.c bias. In other words, if the frequency is low, $\omega \to 0$, the minority carriers follow the a.c signal. Thus,

$$C_{inv} = C_{ox} \qquad for \qquad \omega \to 0 \tag{2.22}$$

If the measurement frequency is very high, $\omega \to \infty$, the minority carriers will not be able to follow the applied signal. The number of minority carriers in the inversion layer therefore remains fixed at its minimum d.c value with depletion width fixed at x_{dmax}. Thus the inversion capacitance is given as:

$$c_{inv} = \frac{C_{ox}}{1 + \frac{\varepsilon_{ox} x_{dmax}}{\varepsilon_{si} t_{ox}}} \tag{2.23}$$

The resultant low frequency and high frequency C-V characteristics of a PMOS capacitor are shown in fig. 2.15.

2.4 The MOSFET

A MOSFET can be viewed as an extension to a MOS capacitor with source (S) and drain (D) regions, generally formed by ion implantation in the substrate, which have an overlap with the gate electrode as shown in fig. 2.16. The source and drain are oppositely doped when compared to the substrate, i.e, if the substrate is p-type then the source and drain are n-type doped and vice versa. The schematic diagram of a MOSFET structure in 2-dimensions and 3-dimensions are shown in fig. 2.16 and fig. 2.17 respectively.

Typical biasing conditions are shown in fig. 2.16. The source is generally connected to the bulk (B) and the bulk is grounded. When the gate of a PMOS capacitor is biased in inversion, the inversion charge layer which is formed just below the oxide-substrate interface creates a high conducting path allowing electrons to flow from the n-type doped source (S) to the n-type doped drain (D). The high conducting region which is formed between the source drain is called as *channel* and the distance between source and drain is known as the *channel length*(L). As the carriers in the channel are electrons, the resulting MOSFET coming from a PMOS capacitor is termed as a *n-channel MOSFET* or *NMOSFET*. Similarly when the substrate is n-type, the MOSFET coming from a NMOS capacitor is termed as *p-channel MOSFET* or *PMOSFET*. A positive voltage is applied to the drain terminal in the case of a NMOSFET and a negative voltage in the case of PMOSFET.

Depending on the applied gate voltage and drain voltage the current flow through the channel from the source to the drain can be controlled. In considering the device geometry the coordinates of the devices are fixed as follows. The x-axis runs from the bottom to the top of the substrate and the y

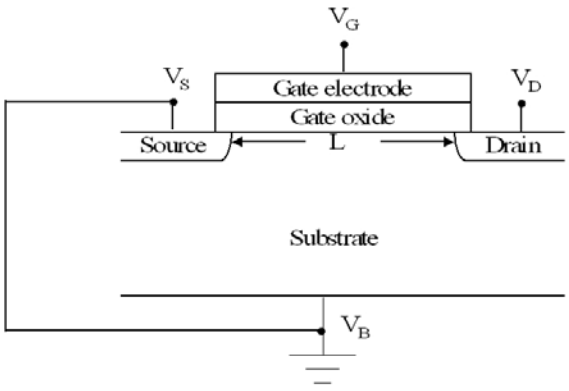

Fig. 2.16: Schematic diagram of a MOSFET in 2-dimension.

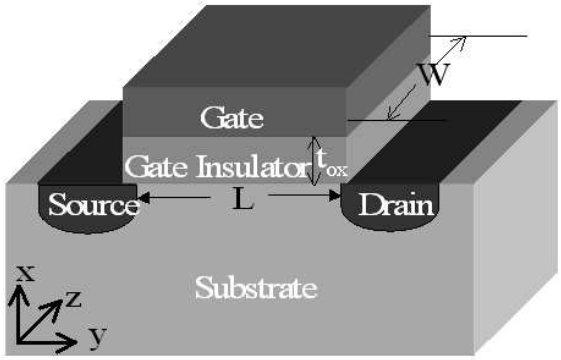

Fig. 2.17: Schematic diagram of a MOSFET in 3-dimension.

axis runs from the left to the right of the device. The source end of the channel is at y = 0, while the drain end of the channel is at y = L. The third axis, z-axis is in to the plane of the paper, along which the device width (W) runs. The area (A) of the device is W × L, which is also the area of the gate.

2.4.1 Threshold Voltage

The definition of the threshold voltage of MOSFETs is similar when compared to the corresponding MOS capacitor [12] and is given as eqn. (2.24).

$$\begin{aligned} V_T &= V_{FB} - 2\phi_f + \frac{Q_d}{C_{ox}} \\ &= V_{FB} - 2\phi_f + \frac{qx_{dmax}N_A}{C_{ox}} \left(1 - \frac{r_j}{L}\left(\sqrt{1 + \frac{2x_{dmax}}{r_j}} - 1\right)\right) \end{aligned} \tag{2.24}$$

where r_j is the junction depth. In long channel MOSFETs, the threshold voltage is identical to its corresponding MOS capacitor as $L \gg r_j$. In short channel MOSFETs, the threshold voltage varies significantly and is discussed in detail in section 2.7.1.1.

2.5 Device Characterization

The MOSFET is characterized by its d.c and a.c characteristics. The d.c characteristics are current-voltage characteristics (I-V characteristics) and the a.c characteristics (obtained from d.c characteristics) are conductance and cutoff frequency. The performance of a MOSFET is dictated by the following factors:

- drain current at given drain and gate bias (I_{DS})
- off-state leakage

- sub-threshold slope (S)
- transconductance (g_m)
- cutoff frequency (f_T)

High performance MOSFETs possess high values for drain currents, transconductance and cutoff frequency, while the values for off-state leakage and sub-threshold slope should be as low as possible. Low leakages means that the device can be used for longer durations where the power supply is limited, for example in the case of mobile applications. A Low sub-threshold slope means that the device has better switching capabilities, which are important for digital circuits. High transconductance and cutoff frequency make the device suitable for radio frequency (RF) applications. In the next following sections, the d.c and a.c characteristics of a MOSFET are discussed in more detail.

2.5.1 I-V Characteristics

The drain current versus drain voltage characteristics (I_{DS}-V_{DS}) are the output characteristics of a MOSFET. The drain current versus drain voltage characteristics (I_{DS}-V_{GS}) of a MOSFET are called subthreshold characteristics. A plot of ln(I_{DS}) versus V_{GS} results in a straight line below V_T. The slope of this line is known as subthreshold slope (S) or subthreshold swing. This section gives a mathematical formalization of drain current and subthreshold slope as a function of gate and drain biases.

2.5.1.1 Drain Current Characteristics

The current in the channel is due to the drift of electrons from the source to the drain. The integration of charge flowing through any cross sectional area of the channel over the channel length gives the total source to drain current I_{DS} [13]. The assumption made in solving the poisson's equation is, the variation of electric field in the y-direction (along the channel) is much less when compared to the electric field variation in x-direction (perpendicular to the channel). This approximation is known as gradual channel approximation (GCA) [14]. The electric field at any point in the channel is given as:

$$E_y = \frac{-dV(y)}{dy} \tag{2.25}$$

The voltage in the channel varies from V_S at y = 0, at the source end to V_D at y = L, at the drain end. The current density in the channel is given as:

$$\begin{aligned} J_{ny} &= q\mu_n n E_y \\ &= -q\mu_n n \frac{dV(y)}{dy} \end{aligned} \tag{2.26}$$

where μ_n is the mobility of carriers in the channel and is explained in section 2.5.1.2. The inversion charge in the channel is given as:

$$Q_{inv}(y) = -q \int_{channel} n(x,y)dx \tag{2.27a}$$

$$Q_{inv}(y) = -q \int_{x=0}^{\infty} n(x,y)dx \tag{2.27b}$$

The current in the channel, flowing from the source to the drain in the channel is the drain current I_{DS}, can be obtained by using eqn. (2.26) as:

$$\begin{aligned} I_{DS} &= -W \times \int_{x=0}^{\infty} J_y dx \qquad\qquad (with J_{ny} < 0) \\ &= -W Q_{inv}(y) \mu_n \frac{dV(y)}{dy} \end{aligned} \tag{2.28}$$

where W is the channel width. The inversion charge in the channel can be obtained by using eqn. (2.11) and eqn. (2.12) as:

$$Q_{inv}(y) = -C_{ox} \left(V_{GS} - V_T + V(y) \right) - Q_B(y) \tag{2.29a}$$

$$Q_B(y) = -\sqrt{2q\varepsilon_{si}\varepsilon_0 N_A \left(2\phi_f + V(y) \right)} \tag{2.29b}$$

By integrating eqn. (2.28) from source to drain, one obtains,

$$I_{DS} \int_0^L dy = -W \mu_n \int_{V_S}^{V_D} Q_{inv}(y) dy \tag{2.30}$$

Using eqns. (2.29), since I_{DS} is constant at any point in the channel, the drain current is given as:

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \int_{V_S}^{V_D} - \left(V_{GS}[V_T + V(y)] - \frac{\sqrt{2q\varepsilon_{si}\varepsilon_0 N_A \left(2\phi_f + V(y) \right)}}{C_{ox}} \right) dV \tag{2.31}$$

If one defines

$$\gamma = \frac{2q\sqrt{\varepsilon_{si}\varepsilon_0 N_A}}{C_{ox}} \tag{2.32}$$

and $V_{DS} \equiv V_D$-V_S, integrating eqn. (2.31) gives

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left(\left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} - \frac{2}{3}\gamma \left(\left(2\phi_f + V_D \right)^{3/2} - \left(2\phi_f + V_S \right)^{3/2} \right) \right) \tag{2.33}$$

The drain current reaches its maximum when the drain voltage reaches a value called "saturation drain voltage", and is obtained by setting $\frac{dI_{DS}}{dV_{DS}} = 0$ into eqn. (2.33) and is given as:

$$V_{DSat} = V_{GS} - V_T + \frac{\gamma^2}{2} - \gamma\sqrt{V_{GS} - V_{FB} + \frac{\gamma^2}{4}} \tag{2.34}$$

The model obtained for I_{DS} and V_{DSat} in eqns. (2.33) and (2.34) is very cumbersome for practical purposes. A simplified model can be obtained by linearizing the maximum depth of the depletion region. The inversion charge from eqn. (2.12) can be written as:

$$\begin{aligned} -Q_B(y) &= \frac{\sqrt{2qN_A\varepsilon_{si}\varepsilon_0 \left(2\phi_f + V(y) \right)}}{C_{ox}} \\ &\cong \gamma\sqrt{2\phi_f} + \delta V(y) \end{aligned} \tag{2.35}$$

Where γ is defined by eqn. (2.32) and δ is a constant that represents the linearized dependency of the depletion charge on V(y). Thus the inversion charge is given as:

$$Q_{inv}(y) = -C_{ox}\left(V_{GS} - V_T - nV(y)\right) \tag{2.36}$$

If one defines

$$n = 1 + \delta \tag{2.37}$$

where "n" is defined as *body factor* or *body effect coefficient*, the drain current can be obtained as

$$I_{DS} = \mu_n C_{ox}\frac{W}{L}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{1}{2}nV_{DS}^2\right) \tag{2.38}$$

and saturation drain voltage is given as:

$$V_{DSat} = \frac{V_{GS} - V_T}{n} \tag{2.39}$$

The saturation drain current is given as:

$$I_{DSat} = \mu_n C_{ox}\frac{W}{L}\frac{\left(V_{GS} - V_T\right)^2}{2n} \tag{2.40}$$

To further simplify the models in eqns. (2.38) - (2.40), if the change in maximum depletion width

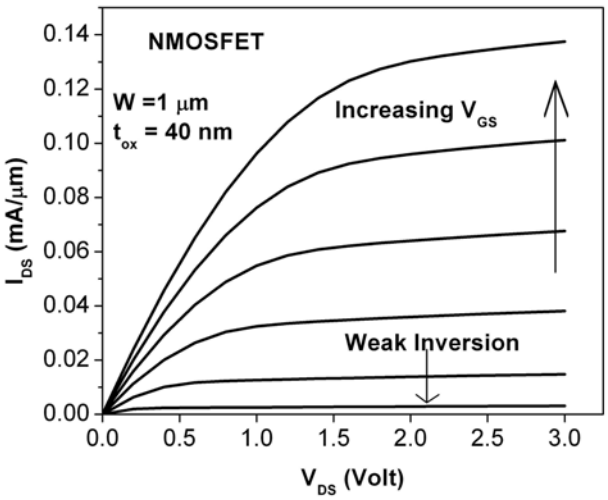

Fig. 2.18: Drain current (I_{DS}-V_{DS}) characteristics of a NMOSFET.

is treated as zero, then eqns. (2.38) - (2.40) become

$$I_{DS} = \mu_n C_{ox}\frac{W}{L}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{1}{2}V_{DS}^2\right) \tag{2.41}$$

and saturation drain voltage is given as:

$$V_{DSat} = V_{GS} - V_T \tag{2.42}$$

The saturation drain current is given as:

$$I_{DSat} = \mu_n C_{ox} \frac{W}{L} \frac{\left(V_{GS} - V_T\right)^2}{2} \tag{2.43}$$

As I_{DSat} varies with the square of drain voltage in saturation, the eqn. (2.43) is called *square law*. The drain current characteristics of a MOSFET are obtained by biasing the gate at a given voltage and then ramping the drain voltage. Typical drain characteristics of a NMOSFET are shown in fig. 2.18.

2.5.1.2 Mobility

The mobility of carriers in a channel represents the ease at which the carriers can move in the channel for a unit of applied electric field. The bulk electron mobility, which is constant throughout the material is μ_{n0}, 1350 cm^2/V-s differs from the hole mobility μ_{p0} 500 cm^2/V-s [15]. The simplest mobility model is the model which assumes the low field mobilities for electrons and holes which is constant throughout the structure and are given as

$$\mu_n = \mu_{n0} \tag{2.44a}$$
$$\mu_p = \mu_{p0} \tag{2.44b}$$

There are different mechanisms which degrade the electron and hole mobilities from the ideal value of n0 and p0. The main effects which reduce the mobility are:

- impurity scattering
- temperature
- surface scattering
- electric fields

The effect of impurity scattering causes a reduction in the carrier mobility with increasing doping as shown in the fig.2.19 [15]. The mobility of carriers impurity scattering is concentration dependent and is given as:

$$\mu_n = \mu_{n0}(N_{total}(x,y)) \tag{2.45a}$$
$$\mu_p = \mu_{p0}(N_{total}(x,y)) \tag{2.45b}$$

where $N_{total(x,y)}$ is the local total impurity concentration in cm^{-3}. As the impurity concentration is temperature dependent, an alternative to concentration-dependent mobility model for carriers is the concentration and temperature dependent analytical mobility models which were discussed extensively in [16],[17], [18].The temperature dependent ionized mobility model estimates the carrier mobility for electrons and holes as [17]:

$$\mu_{LI}(N,T) = a\mu_L(T) + (1-a)\mu_{min} with \tag{2.46a}$$
$$a = \frac{1}{1 + (\frac{T}{300})^b (\frac{N}{N_0})^c} \tag{2.46b}$$

where μ_{min} is 55.24 cm^2/V-s 49.7 cm^2/V-s, b is -3.8 and -3.7, c is -0.73 and -0.7, N_0 is $1.1\times10^{17}cm^{-3}$ and $1.6\times10^{17}cm^{-3}$ for electrons and holes respectively.The carrier mobility which is now being discussed is the bulk mobility in silicon. While considering the carrier transport in a MOSFET, it

occurs in the channel at the oxide-silicon interface. The presence of an interface causes the bulk mobility to degrade. The surface mobility in a MOSFET is significantly lower than the bulk mobility because of the increased scattering of electrons at the oxide-silicon interface [19], [20]. The presence of high electric fields further degrades the mobility. When considering the electric fields and different types of scattering mechanisms, namely,acoustic phonon scattering, surface roughness scattering and

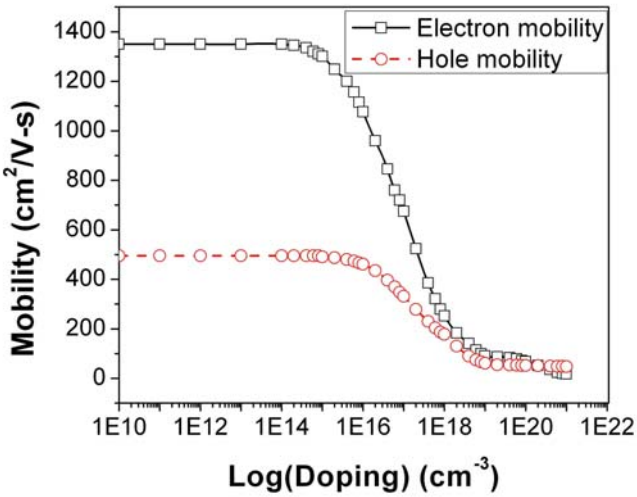

Fig. 2.19: Variation of electron and hole bulk mobility with doping concentration.

Coulombic scattering, a mobility model takes the following form [21], [22]:

$$\mu = f(\mu_{eff}, E_{\parallel}, v_{sat}) + (E_{\perp} - E_0)\frac{df(\mu_{eff}, E_{\parallel}, v_{sat})}{dE_{\perp}} \tag{2.47}$$

For electrons

$$f = \frac{\mu_{eff,n}}{(1 + (\frac{\mu_{eff,n}E_{\parallel}}{v_{sat,n})^2})^{\frac{1}{2}}} \tag{2.48a}$$

$$\mu_{eff,n} = (\frac{1}{\mu_{ph,n}(E_{eff,n})} + \frac{1}{\mu_{sr,n}(E_{eff,n})} + \frac{1}{\mu_{cl,n}})^{-1} \tag{2.48b}$$

$$E_{eff,n} = \frac{E_{\perp} + E_0}{2} \tag{2.48c}$$

For holes

$$f = \frac{\mu_{eff,p}}{1 + (\frac{\mu_{eff,p}E_{\parallel}}{v_{sat,p}})} \tag{2.49a}$$

$$\mu_{eff,p} = (\frac{1}{\mu_{ph,p}(E_{eff,p})} + \frac{1}{\mu_{sr,p}(E_{eff,n})} + \frac{1}{\mu_{cl,p}})^{-1} \tag{2.49b}$$

$$E_{eff,p} = \frac{E_{\perp} + 2E_0}{3} \tag{2.49c}$$

where μ_{eff} is the experimentally measured effective mobility in the inversion layer, E_0 is the transverse electric fields at the edge of the inversion layer, μ_{ph}, μ_{sr} and μ_{cl} are the mobility degradation caused by phonon scattering, surface roughness and Columbic scattering respectively.

2.5.1.3 Subthreshold Slope

The actual dependence of the electron concentration at the surface is an exponential function of surface potential. It is experimentally observed that the drain current below threshold voltage, known as "subthreshold current" is independent of the drain voltage as long as the V_{DS} is larger than a few $\frac{kT}{q}$. This suggests that the subthreshold current is caused by diffusion rather than by drift mechanism. Thus the electron current density from source to drain can be written as

$$\begin{aligned} J_{ny} &= -qD_n\frac{dn}{dy} \\ &= qD_n\frac{n(0)-n(L)}{L} \end{aligned} \tag{2.50}$$

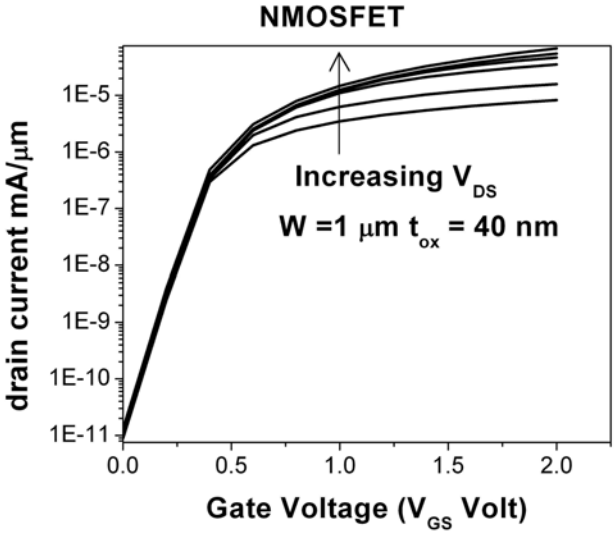

Fig. 2.20: Subthreshold characteristics (I_{DS}-V_{GS}) of a NMOSFET when V_{DS} is greater than a few $\frac{kT}{q}$.

where D_n is the diffusion coefficient for electrons and n(0) and n(L) are electron concentrations at the edge of source and drain junctions are given as

$$n(0) = n\exp\left(\frac{q\phi_s}{kT}\right) \tag{2.51a}$$

$$n(L) = n\exp\left(\frac{q\left(\phi_s - V_{DS}\right)}{kT}\right) \tag{2.51b}$$

where the source is considered at ground and $n = n_i^2/N_A$. The depth of depletion region x_d, through which the current flows is given as

$$x_d = \frac{kT/q}{E_S} \qquad where \tag{2.52a}$$

$$E_S = -\frac{d\phi(x)}{dx}\Big|_{x=0} \tag{2.52b}$$

Using eqns. (2.50) to (2.52) the subthreshold current can be calculated as [13]

$$I_{DS} = \mu_n \frac{W}{L} q \left(\frac{kT}{q}\right)^2 \frac{n_i^2}{N_A}\left[1 - \exp\left(-qV_{DS}/kT\right)\right] \frac{\exp\left(q\phi_s/kT\right)}{\frac{-d\phi_s}{dx}} \tag{2.53}$$

By the definition of subthreshold slope,

$$S = \frac{dV_{GS}}{d\log(I_{DS})} \tag{2.54}$$

From eqns. (2.53) and (2.54) the subthreshold slope can be evaluated as

$$S = \frac{kT}{q}\left(1 + \frac{C_{depl}}{C_{ox}}\right)^{-1} \ln(10) \equiv \frac{kT}{q} n \ln(10) \tag{2.55}$$

where C_{depl} is depletion capacitance. The typical values of the subthreshold slope for bulk CMOS devices is about 80 mV/decade. The Typical subthreshold characteristics of a NMOSFET are shown in fig. 2.20.

2.5.2 A.C. Characteristics

The a.c response of a MOSFET is analyzed using a small signal equivalent circuit, established by a two-port network shown in fig. 2.21(a). At low operational frequencies, the input port between the gate and source is connected across a reverse biased diode inside the structure, which behaves like an open circuit, as represented in fig. 2.21(b). At the output port, the d.c drain current is a function of drain bias (V_{DS}) and gate bias (V_{GS}); that is, $I_{DS} = I(V_{DS}, V_{GS})$. If the a.c drain and gate biases v_{ds} and v_{gs} respectively are added to the d.c drain and gate voltages, assuming that the device can follow the a.c changes in potential quasistatically, the drain current through the structure changes to $I(V_{DS}, V_{GS}) + i_{ds}$, in which i_{ds} is the a.c component of the drain current [8], [23].

Thus,

$$i_{ds} + I_{DS}(V_{DS}, V_{DS}) = I_{DS}(V_{DS} + v_{ds}, V_{GS} + v_{gs}) \tag{2.56}$$

Taylor series analysis of eqn. (2.56) gives the a.c drain current as

$$i_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}}\Big|_{V_{GS}} v_{ds} + \frac{\partial I_{DS}}{\partial V_{GS}}\Big|_{V_{DS}} v_{gs} \tag{2.57}$$

When the operation frequencies are higher, the circuit must be modified to take the capacitive couplings between the gate and source/drain into account. Since the junctions are normally reverse biased, the admittance is equal to the p-n junction depletion capacitances as shown in fig. 2.21(c).

2.5.2.1 Transconductance

The drain conductance (g_d) and transconductance (g_m) are defined from eqn. (2.57) as

$$g_d \equiv \frac{\partial I_{DS}}{\partial V_{DS}}\Big|_{V_{GS}=constant} \tag{2.58a}$$

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}}\Big|_{V_{DS}=constant} \tag{2.58b}$$

The drain conductance can be calculated by using eqn. (2.38) as

$$g_d \equiv \frac{\partial I_{DS}}{\partial V_{DS}}\Big|_{V_{GS}=constant} = \mu_n C_{ox} \frac{W}{L}\left(\left(V_{GS} - V_T\right) - nV_{DS}\right) \tag{2.59}$$

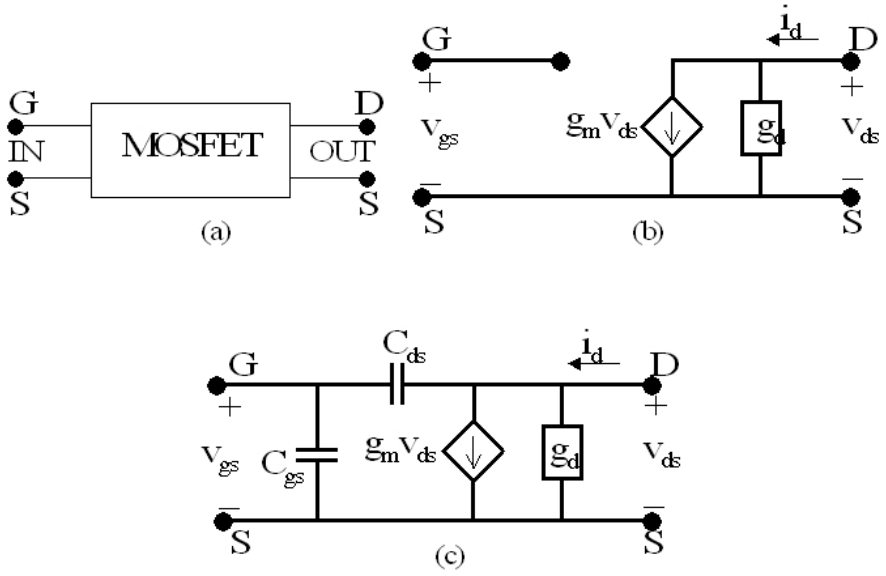

Fig. 2.21: Small signal equivalent circuits of a NMOSFET (a) black box representation (b) low frequency equivalent circuit and (c) high frequency equivalent circuit.

As the drain current is constant in saturation, the saturation drain conductance g_{dsat} is zero in the saturation regime.

The transconductance (g_m) and saturation transconductance (g_{msat}) can be calculated by using eqns. (2.38) and (2.40) as

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}}\Big|_{V_{DS}=constant} = \mu_n C_{ox}\frac{W}{L}V_{DS} \tag{2.60a}$$

$$g_{msat} \equiv \frac{\partial I_{DS}}{\partial V_{GS}}\Big|_{V_{DS}=constant} = \mu_n C_{ox}\frac{W}{L}\frac{V_{GS}-V_T}{n} \tag{2.60b}$$

2.5.2.2 Cutoff Frequency

The cutoff frequency f_T is defined as the frequency where the MOSFET is no longer amplifying the input signal. This means, the frequency at which the ratio between the output current i_{out} and input current i_{in} is, is equal to unity. The output current is given as:

$$i_{in} = j\omega(C_{GS}+C_{GD})v_{gs} \simeq j(2\pi f)C_{ox}v_{gs} \qquad (j=\sqrt{-1}) \tag{2.61}$$

where C_{GD} is assumed to be small when compared to C_{GS} and $C_{GS} \simeq C_{ox}$. Similarly, the output current is given as

$$i_{out} \simeq g_m v_{gs} \tag{2.62}$$

setting $\mid i_{out}/i_{in} \mid = 1$, from eqns. (2.61) and (2.62), the cutoff frequency obtained is:

$$f_T = \frac{g_m}{2\pi C_{ox}} = \frac{\mu_n V_{DS}}{2\pi n L^2} \tag{2.63}$$

The cutoff frequency is an intrinsic property of the device and does not account for any other resistances other than the resistance of the channel. From eqn. (2.63), it can be noted that with a decreasing channel length the cutoff frequency of the device increases.

2.5.3 Measurements

The device characteristics which were discussed earlier can be measured using a prober setup. A prober is used to perform measurements on the hardware performed to characterize the devices. The prober consists of multiple electrodes, which can be connected to various terminals of the devices. In addition to this, the chuck, where the wafer is placed is held at ground potential. Fig. 2.22 shows an optical image of a test structure contact pads which can be connected via pins of a tester to characterize the device.

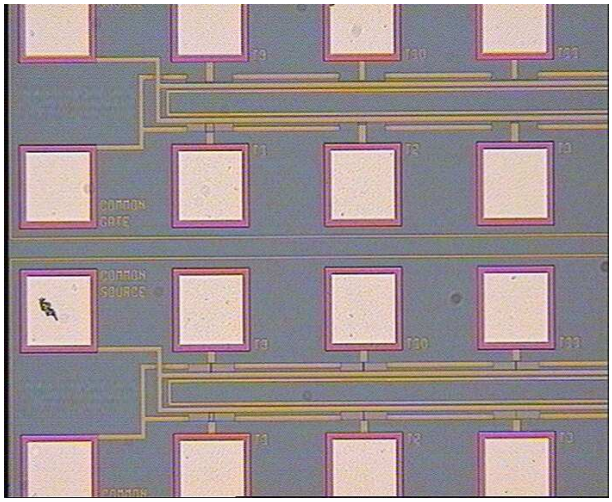

Fig. 2.22: Illustration of a test structure showing common terminals.

2.5.3.1 C-V Measurements

While making the measurements, the substrate was generally grounded and a d.c bias is applied to the gate terminal. A small a.c voltage is applied on the gate and the gate d.c bias varied systematically and the C-V characteristics were recorded.

2.5.3.2 Drain Current Characteristics

While characterizing the MOSFET, the substrate is grounded and all the other voltages applied at drain and gate terminal were measured with respect to the source terminal. However in most cases the source terminal is also grounded. The voltage on the gate terminal is fixed at a certain amount (V_{GS1}) and then the voltage on the drain terminal (V_{DS}) is varied systematically and the source to drain current (I_{DS}) is measured as shown in fig. 2.18. The drain current is plotted against the drain voltage at a given gate voltage. The gate voltage is now changed and fixed at a different voltage (V_{GS2}) and the entire drain current curve is traced.

2.5.3.3 Sub-threshold Characteristics

In tracing the sub-threshold characteristics, the drain voltage is fixed at a given bias with respect to the source and then the gate voltage is ramped. The current from the source to drain is measured. The drain current on a log scale is plotted against the gate voltage at a given bias. The inverse of the slope of the curve gives the sub threshold slope value.

2.6 Surface and Buried Channel MOSFETs

In conventional CMOS devices, the doping concentration of the channel is not always the same as the doping concentration of the bulk. This is due to the fact that various applications need different devices with different threshold voltages. The threshold voltage of a MOSFET is adjusted by implanting dopants in the channel region, thus changing the doping concentration locally. If the threshold voltage of the unimplanted device is too low, a V_T adjust implant with the same type of dopants as the substrate doping type is performed. If the threshold voltage of the unimplanted device is too high, the threshold voltage is pulled down by implanting the opposite kind of species, n-type dopants for a p-substrate and p-type dopants for a n-type substrate. When the V_T adjust implant takes place with opposite dopant atoms, the doping concentration and dopant type in the channel are different when compared to the substrate. This results in devices called *buried channel devices* as shown in fig. 2.23. Due to boron penetration problems [24], n^+ poly silicon gated buried channel PMOSFETs were used in early CMOS technologies. However, these buried channel devices suffer from severe short channel effects and are very difficult to control in sub threshold regime [25].

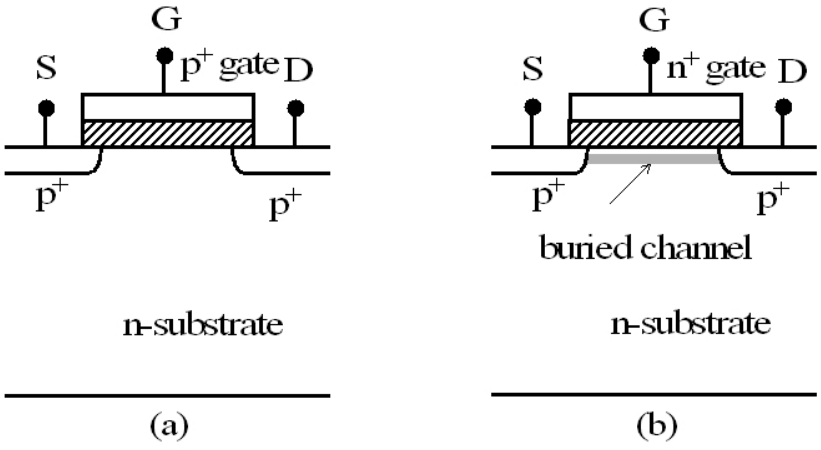

Fig. 2.23: Illustration of PMOSFET (a) surface channel device and (b) a buried channel device.

2.7 MOSFET Scaling

When one observes the dependency of device parameters channel length (L), channel width (W) and gate oxide thickness (t_{ox}) on drain current (eqn. (2.38)), transconductance (eqn. (2.60)) and cutoff frequency (eqn. (2.63)), it is noticeable that when the device parameters are reduced, the performance of the device improves. Decreasing the device parameters L and t_{ox} to obtain a better device performance is known as device scaling. Primarily there are two different types of scaling schemes, namely,

- Constant voltage scaling
- Constant field scaling

In the constant voltage scaling scheme, the voltages in the device are kept constant and in constant field scaling the electric fields in the device are kept constant. When the devices are scaled down according to the constant voltage scheme, the electric fields in the devices increase exponentially causing the device to breakdown and thus a bottleneck for scaling down the device further. Instead,

if devices are scaled down using the constant field scaling scheme [26], [27], the fields are in control and this never leads to a device breakdown, until the physical limits of the device are reached. The effect of the constant field scaling scheme on other important transistor quantities, when the device dimensions channel length (L) and oxide thickness (t_{ox}) are scaled down with a factor κ, are listed below in the table 2.2. In constant field scaling, as the applied voltage is also scaled down,

Quantity	**Scaling Factor**
Device dimensions(L,W,t_{ox},r_j)	$1/\kappa$
Area	$1/\kappa^2$
Packing density (devices per unit area)	κ^2
Doping concentration(N_A)	κ
Bias voltages and V_T	$1/\kappa$
Bias currents	$1/\kappa$
Power dissipation for a given circuit	$1/\kappa^2$
Power dissipation per unit of chip area	1
Capacitances	$1/\kappa$
Capacitances per unit area	κ
Charges	$1/\kappa^2$
Charges per unit area	1
Electric field intensity	1
Body effect coefficient (n)	$1/\sqrt{\kappa}$
Transistor transit time (τ)	$1/\kappa$
Transistor power-delay product	$1/\kappa^3$
Transconductance (g_m)	κ
Cutoff frequency (f_T)	κ^2

Table 2.2: Parameters effected by constant field scaling.

it takes a long time to load the parasitic capacitances, for instance those formed by the metal lines of different metalizing levels. Also as the junction depths of the source and drain are decreased, causing the source and drain resistances to increase. If one considers the slope of $ln(I_{DS})$ versus V_{GS} in weak inversion for a constant V_{DS}, the sub-threshold slope S doesn't scale. For digital circuits it is unwanted, as it makes it difficult to turn on or turn off a device. There are even some drawbacks of the constant field scaling scheme. To avoid extreme cases of constant field scaling and constant voltage scaling, compromising scaling rules have been proposed. One such scaling scheme is, where the geometric dimensions are scaled down according to the constant field scaling but the voltages are scaled less drastically. This is known as *quasi-constant-voltage-scaling*. As the doping is not scaled down, the depletion region widths remain the same. To avoid this, the scaling factor of bulk doping is scaled appropriately, resulting in the *generalized scaling* [28]. Different scaling schemes are tabulated in table 2.3.

When the devices are scaled down, even though the device performance improves, scaling introduces undesired effects. The effects of scaling can be divided into two categories, namely:

- short channel effects
- gate stack effects

	Scaling Factor			
Quantity	**Constant field scaling**	**Constant voltage scaling** $1< \kappa' < \kappa$	**Quasi-constant voltage scaling** $1< \kappa' < \kappa$	**Generalized scaling** $1< \kappa' < \kappa$
W,L	$1/\kappa$	$1/\kappa$	$1/\kappa$	$1/\kappa$
t_{ox}	$1/\kappa$	$1/\kappa'$	$1/\kappa$	$1/\kappa$
N_A	κ	κ	κ	κ^2/κ'
V_{DS},V_T	$1/\kappa$	1	$1/\kappa'$	$1/\kappa'$

Table 2.3: Scaling rules for CMOS devices.

2.7.1 Short Channel Effects

The short channel devices differ from long channel devices in many ways. The basic features that short channel devices encounter and should be considered while designing a device are:

1. short-channel effect (V_T roll-off)
2. velocity saturation
3. channel length modulation
4. source-drain series resistance
5. MOSFET breakdown

2.7.1.1 Short-channel Effect (V_T roll-off)

The short-channel effect is the decrease in MOSFET threshold voltage when the channel length is reduced and is termed as V_T roll-off [13], [29]. In long channel devices, the shape of the depletion charge layer in the channel resembles a rectangular shape. While in short channel devices, due to the drain and source junction penetrations, the shape of the depletion charge can be approximated as a trapezium, as shown in fig. 2.24. When the devices are scaled down more aggressively, the

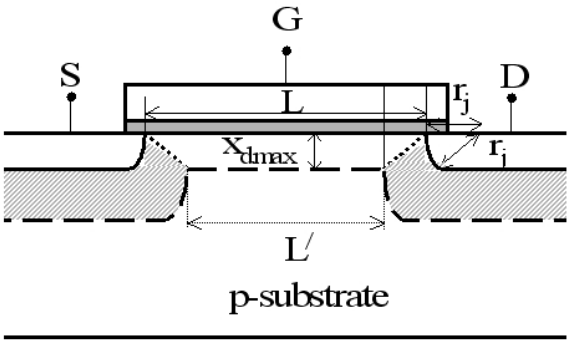

Fig. 2.24: Schematic diagram of a MOSFET illustrating the charge sharing model of the inversion charge.

shape of the depletion charge changes into a triangular shape. This results in a reduced inversion charge in the channel due to the penetration of junctions into the channel region. If $L^{'}$ is the distance

between the source and drain junctions at a distance x_{dmax} from the oxide-substrate interface, then the threshold voltage of a MOSFET is thus given by eqn. (2.64).

$$\begin{aligned} V_T &= V_{FB} + 2\phi_F + \frac{Q_d}{C_{ox}} \\ &= V_{FB} + 2\phi_F + \frac{qx_{dmax}N_A}{C_{ox}} \left(1 - \frac{r_j}{L}\left(\sqrt{1 + \frac{2x_{dmax}}{r_j}} - 1\right)\right) \end{aligned} \tag{2.64}$$

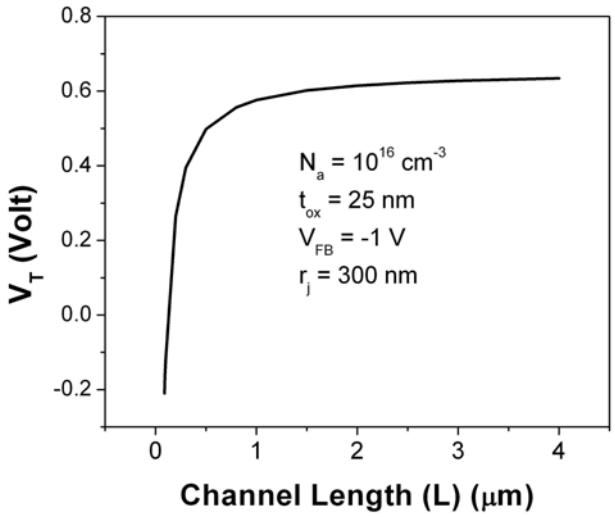

Fig. 2.25: Threshold voltage roll off in a MOSFET due to the short channel effect.

In short channel devices, as the channel length decreases and the charge sharing in the channel increases, the factor in the parenthesis of eqn. (2.64) reduces significantly reducing the threshold voltage when compared to its long channel equivalent. Fig. 2.25 illustrates the threshold voltage of a MOSFET as a function of channel length. The reduction in threshold voltage for a MOSFET as a function of channel length is given as:

$$\Delta V_T = -\frac{qx_{dmax}N_A}{C_{ox}}\frac{r_j}{L}\left(\sqrt{1 + \frac{2x_{dmax}}{r_j}} - 1\right) \tag{2.65}$$

In order to improve the V_T of the device a V_T adjust implantation is generally performed in the channel to improve the doping locally in the channel.

2.7.1.2 Drain Induced Barrier Lowering (DIBL)

When the MOSFET is in off state, the potential barrier (p-type region) between source and drain (to electrons in a NMOSFET) prevents the electron flow from the source to drain. The potential barrier and the surface potential are mainly controlled by the gate voltage. In long channel devices, the potential barrier is flat and only the drain and source fields effect the channel at its very ends. However, in the case of short-channel devices, the drain and source fields penetrate deep into the middle of the channel as illustrated in fig. 2.26 [30], and lowers the potential barrier between the source and drain [25], [31]. This causes a substantial increase in subthreshold current and as a result

the threshold voltage decreases. When source and drain are biased, the potential barrier decreases further. The barrier is induced because of drain bias, this effect is termed as Drain Induced Barrier Lowering (DIBL). The magnitude of DIBL is defined by the following relationships

$$DIBL(Volt) = V_T\Big|_{V_{DS1}} - V_T\Big|_{V_{DS2}} \tag{2.66a}$$

$$DIBL = \frac{V_T\Big|_{V_{DS1}} - V_T\Big|_{V_{DS2}}}{V_{DS1} - V_{DS2}} \tag{2.66b}$$

The shift in V_T caused by DIBL for a short channel device is given as

$$\Delta V_T = 8(m-1)\sqrt{\phi_{bi}(\phi_{bi} + V_{DS})}e^{-\pi L/(x_{dmax}+3t_{ox})} \tag{2.67a}$$

$$m = 1 + \frac{3t_{ox}}{x_{dmax}} \tag{2.67b}$$

where ϕ_{bi} is the built in potential of the source or drain to substrate junction. When the device is made very short or the drain voltage is high, the devices reach the *punch-through* condition, where

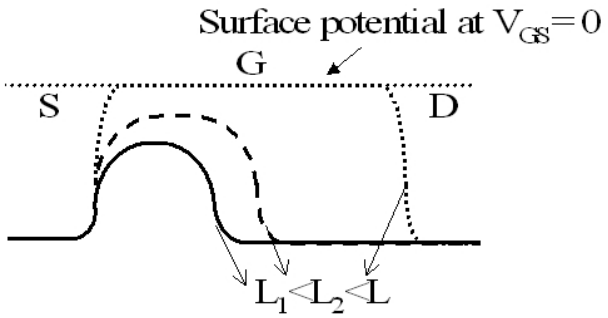

Fig. 2.26: Distribution of surface potential in the channel of MOSFETs with different channel lengths at a given gate bias. The reduction in surface potential is due to DIBL.

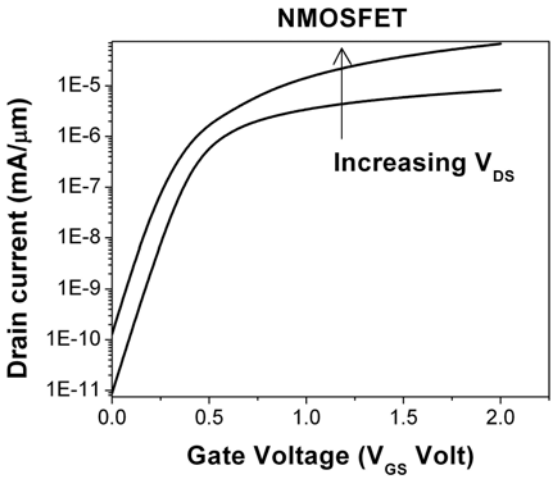

Fig. 2.27: Degradation of subthreshold slope due to DIBL.

the gate totally loses control of the channel and the surface potential is more controlled by the drain rather than the gate and high drain currents persist independent from the gate voltage. As a result, the subthreshold slope increases and V_T decreases as shown in fig. 2.27. In order to reduce DIBL, a DIBL implant is performed, which generally differs from a V_T adjust implant.

2.7.1.3 Velocity Saturation

In long channel devices, when the drain voltage is increased, the drain current firstly increases and then saturates at a voltage equal to $V_{DSat} = (V_{GS} - V_T)/n$ with the onset of pinch off at the drain. In short channel devices, the drain current may saturate at lower voltages due to velocity saturation [32], [33], [34]. This is due to the high fields in the channel, which cause the carrier velocity to saturate. The drain saturation current caused by velocity saturation is given as

$$I_{DSat} = \mu_n C_{ox} \frac{W}{L\left(1 + \frac{V_{DS}}{LE_C}\right)} \frac{(V_{GS} - V_T)^2}{2n} \tag{2.68}$$

where E_C is the critical electrical field in the channel. Thus when velocity saturation is taken into account, the saturation drain current decreases.

2.7.1.4 Channel Length Modulation

When a long channel device is biased beyond saturation, the drain current remains constant [27]. In contrast, the drain current in a short channel device increases as the effective channel length decreases as shown in fig. 2.28. When the drain voltage is increased beyond V_{DSat}, the saturation

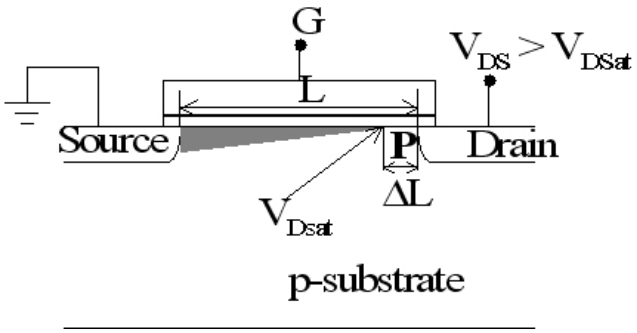

Fig. 2.28: Schematic diagram of channel length modulation. Due to the drain bias, a depletion region is extended into the channel region thus reducing the channel length.

point where the surface channel collapses shifts slightly towards the source resulting in a reduced channel length. The effect of channel length modulation can be observed with an increment in saturation drain current (I_{DSat}). The increase in the saturation current in a short channel device is given as

$$I_{DSat}(shortchannel) = \frac{I_{DSat}}{1 - (\Delta L/L)} \tag{2.69}$$

The channel length modulations result in a non-zero drain conductance value, as with the saturation, the drain current still increases because of channel length modulation.

2.8 Gate Stack Effects

According to the scaling rules, with scaling of lateral device dimensions, the gate oxides should be scaled down as well. The main reason in scaling down a device is achieving ultra thin oxides for gate isolation. If the oxide is not thick enough, the carriers can tunnel through the oxide and can cause device failure. Different leakage currents because of the direct tunneling through the gate oxide increase exponentially with gate oxide thickness t_{ox} and may exceed the on state current. On the other hand, with decreasing gate oxide thickness the device off-state currents also increase, thus the devices need more static power and they contradict low-power application requirements. Gate and off state leakage currents aspiring from the gate oxide thinning are summarized in fig. 2.29[35].

In order to reduce the gate leakages, the physical thickness of the gate dielectric has to be increased. The physical thickness can be increased while keeping the electrical thickness constant. This can be achieved by introducing high-K gate dielectric as a gate dielectric.

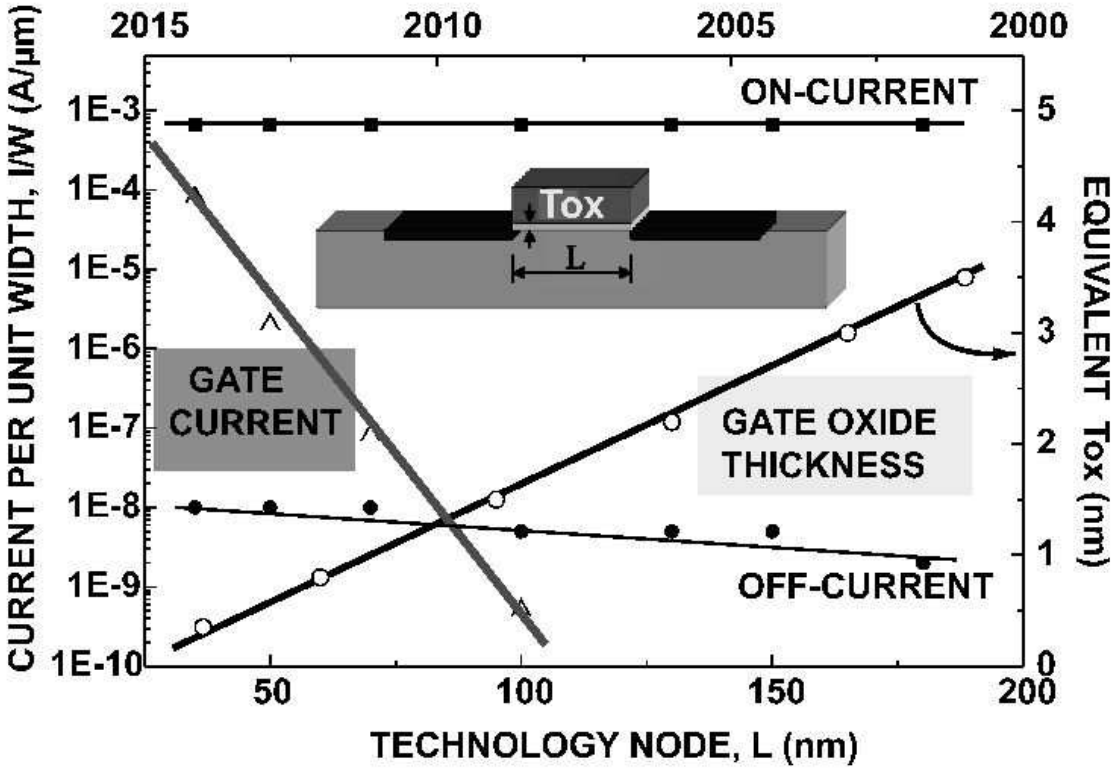

Fig. 2.29: A comparison of leakage currents with "ON" current in highly scaled MOSFETs.

2.8.1 High-K Gate Dielectrics

When a high-K gate dielectric is used, instead of SiO_2 as the gate dielectric, the physical thickness of the gate dielectric can be increased while keeping the gate capacitance constant. This can be explained in the following fashion. The gate oxide capacitance is given as

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}} \tag{2.70}$$

When a high-K gate dielectric is used as the gate insulator, the gate capacitance is given as

$$C_K = \frac{\varepsilon_0 \varepsilon_K}{t_K} \tag{2.71}$$

where ε_K is the relative dielectric constant of the high-K material under consideration. Comparing eqns. (2.70) and (2.71),

$$\frac{C_{ox}}{C_K} = \frac{\varepsilon_K t_{ox}}{\varepsilon_{ox} t_K} \tag{2.72}$$

If C_{ox} and C_K are equal then from eqn. (2.72), we get

$$t_K = \frac{\varepsilon_K t_{ox}}{\varepsilon_{ox}} \tag{2.73}$$

As $\varepsilon_K > \varepsilon_{ox}$, $t_K > t_{ox}$. This means that the physical thickness of the oxide can be increased by a factor of $\varepsilon_K/\varepsilon_{ox}$, still keeping the gate dielectric capacitance fixed at C_{ox} when a high-K gate

dielectric material is used as gate insulator instead of SiO_2. The gate oxide thickness is now known as equivalent electrical oxide thickness or simply Equivalent Oxide Thickness (EOT) is given by eqn. (2.74) and can be seen in fig. 2.30.

$$EOT = \frac{\varepsilon_{ox}}{\varepsilon_K} t_K \tag{2.74}$$

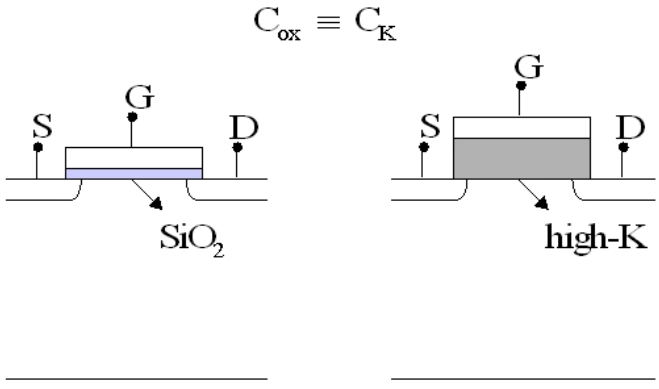

Fig. 2.30: Schematic diagram of a MOSFET illustrating the variation of physical thickness caused by the introduction of a high-K stack. The EOT and gate oxide capacitance are equal for both cases.

The important high-K materials which are prominent and that can potentially replace SiO_2 are listed below in table 2.4 [36], [37], [38]. The integration of high-K materials comes with severe

High-K Material	ε_K
Aluminum Oxide (Al_2O_3)	10
Zirconium Oxide (ZrO_2)	20
Hafnium Oxide (HfO_2)	22
Tantalum Oxide (Ta_2O_5)	25
Praseodimium Oxide (Pr_2O_3)	30
Cesium Oxide (CeO_2)	52
Titanium Oxide (TiO_2)	60
Strantium-Titanium Oxide ($SrTiO_3$)	100

Table 2.4: Dielectric constants of different High-K materials.

problems and they suffer from lots of disorders like charge trapping [39], V_T shift [40], reaction with poly gate, fermi level pinning [41], [42] and disability to high temperature processing steps and mobility degradation [43], [44], to mention some. However solutions are being found to the problems mentioned above, for which SiO_2 can be replaced [45].

2.8.2 Gate Depletion

The gate of a MOS device is generally fabricated by depositing poly silicon with very high doping levels of 10^{20} atoms cm^{-3}. When the gate is biased, the gate poly silicon depletes due to the polarity of the biasing voltage. This results in a decrease of gate oxide capacitance and reduces the drain current. The poly gate depletion is explained in detail in later sections.

2.8.2.1 Poly Gate Depletion Effect

In conventional CMOS devices, the gate is symmetrically doped when compared to source and drain. This means, in a NMOSFET, the gate is doped with n^+ type dopants and in a PMOSFET, the gate is doped with p^+ type dopants as shown in fig. 2.31. The degenerately doped poly gates have a good conductivity almost comparable to the conductivity of metal gates.

When the device is in "ON" state, the n^+ gate of a NMOSFET is biased with a positive voltage and the p^+ gate of a PMOSFET is biased with a negative voltage. The gate biasing in the case of the poly is such that the gate voltage polarity is opposite to the poly gate doping type. This biasing results in the formation of a depletion region in the gate at the poly gate-gate oxide interface as shown in fig. 2.32. Schematic illustration of gate depletion and the resultant gate capacitance are shown in fig. 2.32(a) and fig. 2.32(b) respectively. The resultant band diagram of the n^+ poly gate region of this type of NMOSFET is shown in fig. 2.33.

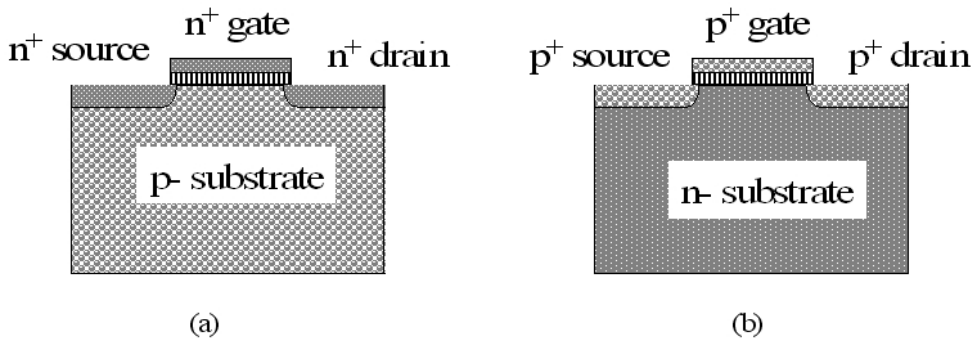

Fig. 2.31: Schematic description of gate electrode in conventional CMOS devices, showing (a) a n^+ poly gate of a NMOSFET and (b) a p^+ poly gate of a PMOSFET.

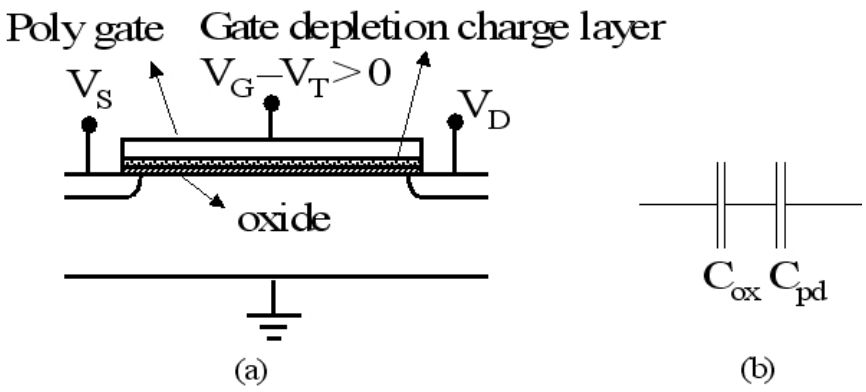

Fig. 2.32: Schematic representation of (a) poly gate depletion in a conventional CMOS devices and (b) equivalent capacitance representation of the gate capacitance when the poly gate is depleted.

When the doping concentration of the gate is 10^{20} cm^{-3}, using eqn. (2.10) the depletion width caused by poly gate depletion can be calculated as 4nm. This depletion region behaves as a capacitor,

known as Poly Gate Depletion Capacitance (PGDC, C_{pd}). The PGDC is in series with the gate oxide capacitance. As a result, the resultant gate capacitance C_G decreases and is given as:

$$\frac{1}{C_G} = \frac{1}{C_{ox}} + \frac{1}{C_{pd}} \tag{2.75}$$

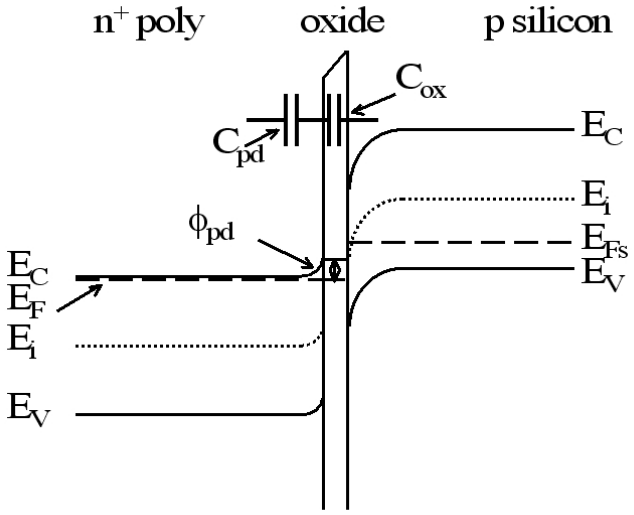

Fig. 2.33: Band diagram illustrating poly gate depletion effect when a positive gate voltage is applied to the degenerately doped n^+ poly silicon gate of a NMOSFET (PMOSC). The applied gate bias results in an upward band bending indicating the presence of the depletion region.

As the device scaling demands the scaling down of EOT, the only possible solution to improve the gate capacitance is to increase the gate doping. Even though the gate is degenerately doped, however, due to process limitations and dopant diffusion caused by high temperature processing steps, which are necessary for dopant activation, the gate doping at the gate poly-gate oxide interface decreases. As a result, a finite depletion region still exists and even though the gate depletion is reduced it is not fully eliminated, which can be seen from the C-V characteristics shown in fig. 2.34.

When the gate oxide is sufficiently thick, the gate depletion region can be neglected and the gate capacitance returns to its maximum value C_{ox}. When the gate oxide thickness is scaled down, the contribution from $1/C_{ox}$ from eqn. (2.75) decreases and the contribution from $1/C_{pd}$ can no longer be neglected. As a result, the resultant gate capacitance decreases, as shown in fig. 2.34. The degradation caused by poly gate depletion results in a voltage drop across the gate electrode [5].

In order to reduce poly gate depletion, the poly gate doping should be increased. This results in a thinner depletion region width in the poly gate and as a result the contribution from poly gate depletion capacitance decreases, thus improving the gate capacitance. When the equivalent gate oxide thickness is scaled down, the contribution from the C_{ox} term in eqn. (2.75) reduces, thus the poly gate depletion capacitance again contributes significantly. In order to make poly-depletion effects negligible, C_{pd} must be sufficiently greater than C_{ox}. This can be achieved in two ways as shown in fig. 2.35. Firstly, for a given oxide thickness t_{ox}, by increasing the poly-silicon doping concentration which makes the C_{pd} to increase as the depletion region width in the poly silicon decreases. Alternatively by increasing t_{ox} for a given gate doping concentration, which causes the C_{ox} to decrease. Because of this the only possible solution is to increase the gate doping of the poly

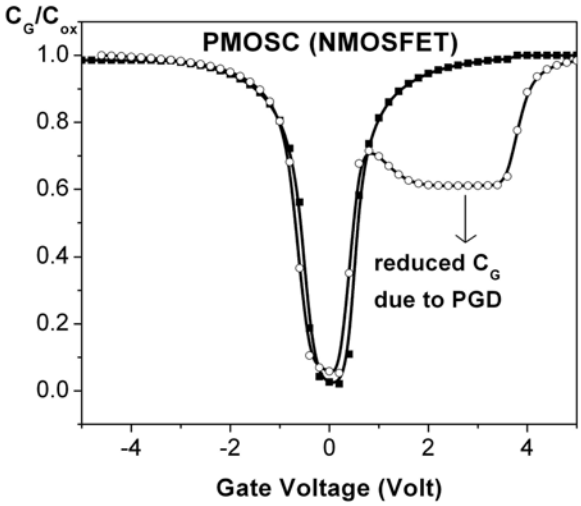

Fig. 2.34: Degradation of gate capacitance in a PMOSC (NMOSFET) caused by poly gate depletion. The gate was doped degenerately with a doping concentration of 10^{20} cm^{-3}.

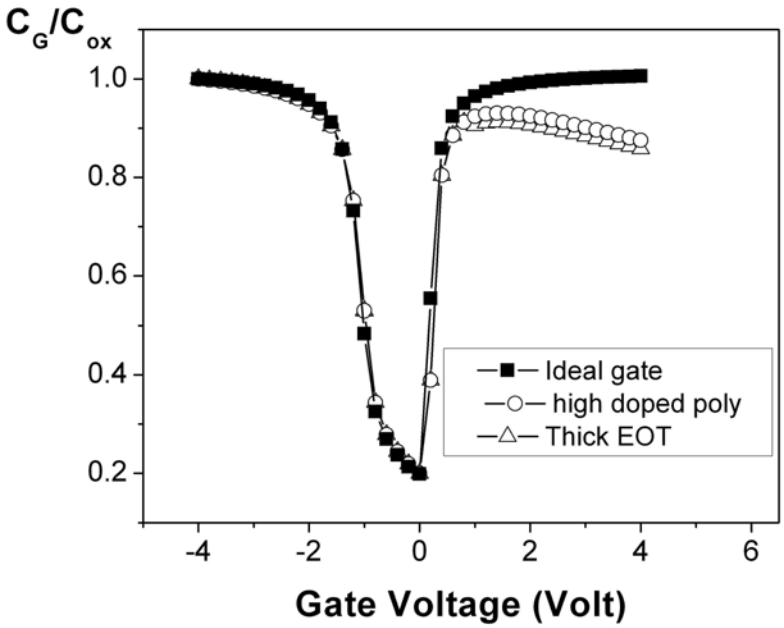

Fig. 2.35: Improvement in C_G, which can be achieved by highly doped poly gate or by increasing EOT.

gate electrode as any particular technology node determines the oxide thickness. Thus if the poly gate is not doped enough or the oxide thickness is too small, it leads to a reduced inversion charge density in the channel and finally more importantly degradation of transconductance of the MOSFET [46], [47].

In ultra thin oxide systems, where the gate oxide thickness is less than 3 nm, even if the gate is degenerately doped, the gate oxide capacitance decreases significantly. The degradation of gate capacitance for various EOT is illustrated in fig. 2.36. When the gate is very highly doped, table 2.5 gives an estimation of reduction in C_G in % caused by poly gate depletion. Thus in modern CMOS devices, when the devices are scaled down, the poly gate depletion plays a major role.

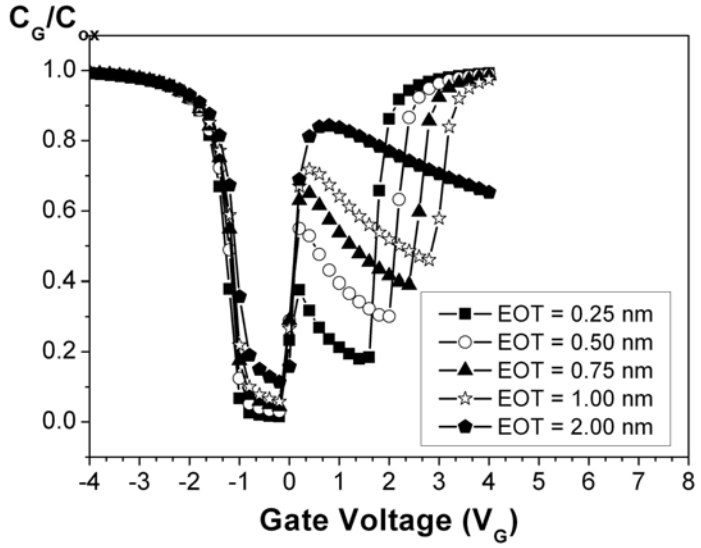

Fig. 2.36: Degradation of gate capacitance C_G due to scaling of EOT.

When the device performance is taken into account, the parasitic charge layer effects the inversion layer charge density in a MOSC or a MOSFET. The increment in the gate voltage increases the parasitic charge centers at the interface, which means that part of the applied gate voltage is screened by the gate depletion charge. As a result, the inversion layer charge decreases in the presence of poly depletion and as a consequence of this, the drain current decreases in a MOSFET. The abrupt raise

EOT (nm)	C_{ox} (F/cm^2)	C_G (F/cm^2)	% reduction in C_G
10	3.45×10^{-7}	3.42×10^{-7}	< 1
4	8.63×10^{-7}	7.76×10^{-7}	8
2	1.73×10^{-6}	1.42×10^{-6}	16
1	3.45×10^{-6}	2.17×10^{-6}	36
0.75	4.60×10^{-6}	2.43×10^{-6}	44
0.5	6.92×10^{-6}	2.68×10^{-6}	61
0.25	1.39×10^{-5}	3.34×10^{-6}	76

Table 2.5: Degradation of gate capacitance (C_G) in a MOSFET with decreasing EOT.

in the capacitance in the C-V curves (fig. 2.36), is due to the inversion of the poly silicon-oxide interface [46]. From the device characteristics of bulk CMOS devices (sec. 2.5.1) and FD SOI devices (sec. 3.4), the saturation drain current is directly proportional to the C_{ox} (eqns. (2.40) and (3.16)). In the presence of poly gate depletion, C_{ox} should be replaced by the total gate capacitance C_G. The reduction in C_G from its maximum value C_{ox} leads to a reduction in drain current and saturation

drain current I_{DSat}. As the sub threshold slope is inversely proportional to the gate capacitance, the subthreshold slope also increases, which degrades the device off-state leakage due to less control over the channel which is caused by gate depletion. The effective equivalent oxide thickness due to the poly gate depletion when the EOT is scaled down is summarized in table 2.5.

The effect of poly gate depletion, which is not predictable, raises due to the presence of the parasitic charges in the high density parasitic charge layer near the poly silicon-oxide interface. These parasitic charges at the gate electrode-gate oxide interface cause the carriers in the channel to scatter. This effect which is known as remote Coulomb scattering. The effect of the scattering of charge carriers is discussed in the next section.

2.8.3 Remote Coulomb Scattering

In section 2.8.2.1, it was mentioned that, to avoid the capacitive effects of poly-depletion as the oxide thickness is reduced, the use of highly doped poly-silicon gate [48] results in a high density charge layer. The combination of a very thin oxide and a high poly-silicon doping concentration could result in a large degree of remote Coulomb scattering (RCS) of channel electrons by the poly depletion charge and may cause a substantial amount of mobility degradation [49], [50], [51] [52] [53], [54]. Apart from RCS, an important long-range Coulomb interaction between the channel and the heavily doped source/drain/gate (electronplasmon interaction) [55] also strongly reduces the electron mobility for oxides thinner than 3 nm.

When the poly silicon gate is doped at very high doping concentration levels, despite the width of the gate depletion region decreasing, the highly doped gate results in a highly dense parasitic charge layer at the poly silicon gate-gate oxide interface as illustrated in fig. 2.37. These parasitic charges were not screened by the thin oxides thus resulting in the scattering of charge carriers in the channel. Even though the parasitic gate charges are present in thick oxide systems, the thick oxide can screen

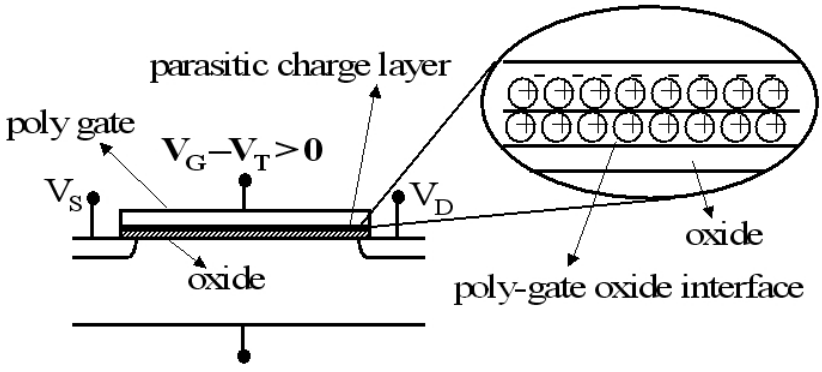

Fig. 2.37: Schematic representation of a high dense parasitic charge layer in a conventional CMOS device due to poly gate depletion.

the parasitic charges and as a result the scattering of carriers is not present in thick oxide systems. Thus, RCS is a thin oxide system phenomenon. The parasitic charges, through the scattering of carriers in the channel cause the mobility degradation. Thus the mobility can now be written as

$$\frac{1}{\mu_{n,p}} = \frac{1}{\mu_l} + \frac{1}{\mu_i} + \frac{1}{\mu_{RCS}} \tag{2.76}$$

where μ_{RCS} is the mobility caused by RCS. Thus the effect of RCS is mobility degradation of carriers in the channel. As a consequence, the reduced mobility degrades the device performance, in terms of I_{Dsat}, g_m and f_T. The subthreshold slope is not severely effected because of its logarithmic dependency on mobility.

In order to reduce RCS, one should have very little charge density or even zero charge density at the poly silicon-gate oxide interface. In conventionally doped poly silicon gates, this can be achieved by reducing the gate doping concentration. The reduced gate doping concentration results in poly depletion effects, which degrade the device performance severely. Thus from the viewpoints mentioned above it is obvious that both poly gate depletion and RCS are unavoidable in conventionally doped gates when the devices are scaled down into sub 100 nm regime.

In the sections that follow the gate architectures will be discussed, which will allow the poly gate depletion effects to be eliminated, and consequently the RCS.

2.9 Parasitic Device Capacitances

In bulk CMOS devices, the parasitic capacitances play an important role in device performance towards RF applications [23]. Apart from the parasitic capacitances, caused by high but finite resistivity of silicon substrate, different parasitic transistor combinations are possible via bulk in CMOS devices. These parasitic transistors can lead to latch-up problems in the CMOS devices. Table 2.6 lists important parasitic capacitances in a CMOS device and are illustrated in fig. 2.38.

Capacitance	**V_G<V_T**	**Non Saturation**	**Saturation**
C_{Gsub}	W×L×C	0	0
C_{GS}	C_{ov}	$C_{ov}+\frac{1}{2}W \times L \times C_{ox}$	$C_{ov}+\frac{2}{3}W \times L \times C_{ox}$
C_{GD}	C_{ov}	$C_{ov}+\frac{1}{2}W \times L \times C_{ox}$	C_{Dsub}
C_{Ssub}	PN junction capacitance	PN junction capacitance	PN junction capacitance
C_{Dsub}	PN junction capacitance	PN junction capacitance	PN junction capacitance

Table 2.6: Parasitic capacitances in a MOSFET.

In bulk CMOS devices, the source to substrate (C_{Ssub}) and drain to substrate capacitances (C_{Dsub}) are simple PN junction capacitances. If the gate voltage is positive but lower than the threshold voltage, the gate to substrate capacitance (C_{Gsub}) is equal to W×L×C, where C is the capacitance of the MOS capacitor in depletion. Above V_T, the inversion layer acts as a shield between the gate and substrate and as a result C_{Gsub} is zero. The gate to source C_{GS} and gate to drain capacitance C_{GD}, both are equal to the overlap capacitance C_{ov}.

Although the parasitics capacitances and transistors even though cannot be completely eliminated, they can be reduced if the bulk of the silicon is replaced by an insulating low dielectric constant material. If bulk silicon, where the transistor action does not take is replaced by SiO_2,the substrate capacitances can be lowered because of the less dielectric constant of SiO_2, resulting in SOI MOSFET (Silicon On Insulator) devices.

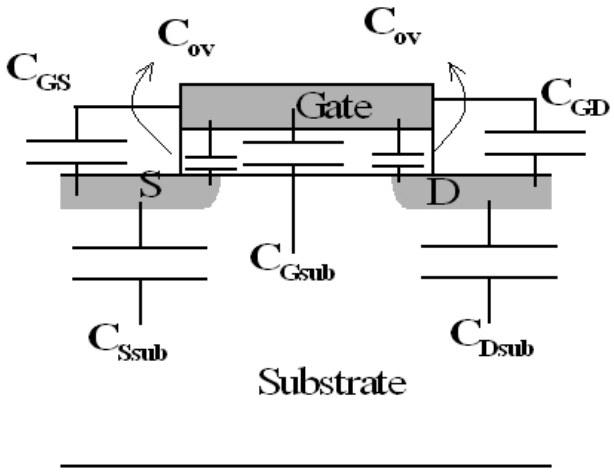

Fig. 2.38: Schematic diagram of parasitic capacitances in a MOSFET.

2.10 Conclusions

In this chapter, the functioning of a MOSFET by using a MOS capacitor electrostatics has been discussed. The device characteristics of MOSFET namely I-V characteristics, and a.c characteristics were discussed. Scaling MOSFET results into short channel effects which can degrade the device performance and their effects were discussed. The different variation of the bulk MOSFET, a SOI MOSFET will be talked about in the next chapter along with its device characteristics.

3

Silicon On Insulator MOSFET

3.1 Introduction

The MOSFET is a surface device, where the carrier transport takes place in the top of the device at gate oxide-substrate interface. Apart from this, the main purpose of the silicon substrate in bulk CMOS devices is to provide mechanical support for the devices. The bulk silicon apart from providing the mechanical support, introduces numerous parasitics, as discussed in the previous chapter. In order to give mechanical support and simultaneously reduce the parasitics, the bulk silicon in bulk CMOS devices is replaced by a two layered structure, an oxide beneath the active device area, called *Buried Oxide*, or simply BOX, and a silicon substrate to support the oxide layer. The presence of BOX underneath the devices not only reduces the junction capacitances but also other capacitances like poly gate to substrate and the capacitances raising from metal lines [56]. Thus the Silicon On Insulator MOSFETs (SOI MOSFET) are substantially different to the bulk MOSFETs. Generally, the thickness of the silicon film, where the active devices are fabricated ranges from 20 to 200 nm and the BOX layer ranges from 80 to 400 nm. In the sections that follow, variations of SOI device depending upon the silicon film thickness are discussed. Furthermore, the electrical characteristics of SOI devices are explained.

3.2 Fully and Partially Depleted SOI MOSFETs

The physics of SOI MOSFETs is highly dependent on the thickness and doping concentration of the silicon film. Two possible device configurations can be distinguished, when the devices are biased in inversion: devices in which the silicon film in the channel region is never completely depleted, are called *Partially Depleted SOI (PDSOI) MOSFETs* and devices in which the silicon film in the channel region is always completely depleted, are called *Fully Depleted SOI (FDSOI) MOSFETs*. A schematic representations of PDSOI and FDSOI MOSFETs are shown in fig. 3.1. From looking at fig. 3.1, it is noticeable that a SOI MOSFET possesses two interfaces, namely a front interface, and a back interface, which is connected to the bulk of silicon. The depletion width in a silicon film can be calculated as

$$x_{dmax} = \sqrt{\frac{4\varepsilon_0 \varepsilon_{si} \phi_f}{qN_A}} \tag{3.1}$$

where $\phi_f = -\big(kT/q\big)\ln\big(\frac{N_A}{n_i}\big)$. If the thickness of silicon film (t_{si}) is larger than twice the value of the depletion width (x_{dmax}), then there is no interaction between the depletion zones arising from the front and back interfaces. A neutral region exists between the two depletion regions as shown in the diagram in fig. 3.1(a). This neutral region is called *body*, and is connected to the ground through

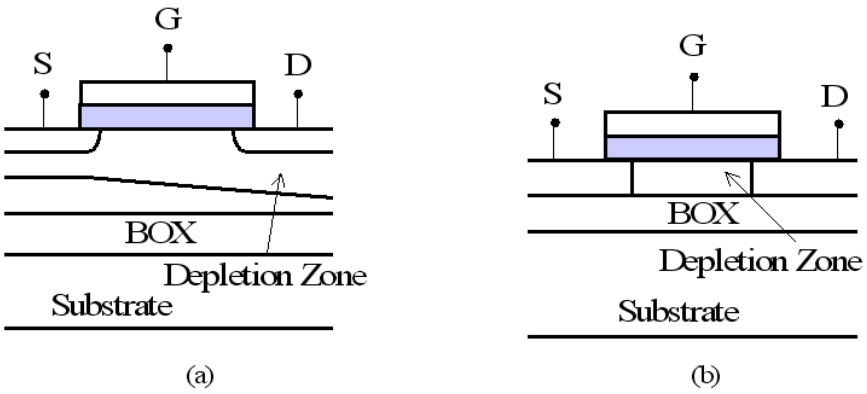

Fig. 3.1: Schematic diagram of a (a) partially depleted SOI MOSFET and (b) fully depleted SOI MOSFET.

a body contact. The device characteristics of such PDSOI CMOS devices are very similar to the characteristics of bulk CMOS devices. However, if the body is left electrically floating, the PDSOI devices suffer from major setbacks, called *floating body effects* [57]. In addition, a lateral parasitic open base NPN bipolar transistor may be formed between the n^+ source, p-type substrate and n^+ drain regions in the case of a SOI-NMOSFET and a PNP open base bipolar transistor in the case of a SOI-PMOSFET, which severely influences the device characteristics [58].

In a FDSOI device, the thickness of silicon film (t_{si}) is smaller than x_{dmax}. In such a case, when the front gate is biased at threshold voltage, the silicon film is fully depleted irrespective of the back gate bias. The energy band diagram of a FDSOI device when the front and back gates are biased in inversion is shown in fig. 3.2. The performance, as discussed in section 2.5, still stands even in the case of FDSOI and PDSOI devices. The interesting properties of SOI devices raise from the back gate biasing conditions. As the back gate biases in PDSOI devices have less effect due to high silicon thickness above the BOX, the most attractive device characteristics raise from the back gate bias of the FDSOI devices. These will be discussed in the sections that follow.

The presence of front and back interface in a FDSOI device gives nine different biasing conditions depending on the accumulation, depletion and inversion biasing of the front and back interfaces [59]. In all these biasing conditions, the important biasing conditions which are of practical importance are when

- the silicon film at the front gate is in inversion and the silicon film at the back gate is in depletion
- the silicon film at the front gate is in depletion and the silicon film at the back gate is in depletion

In addition to the conditions mentioned above, the back interface near the source and drain ends can be locally accumulated or depleted depending upon the drain and source bias voltages. In the following analysis, a subscript "1" represents the front gate while a subscript "2" represents the back gate.

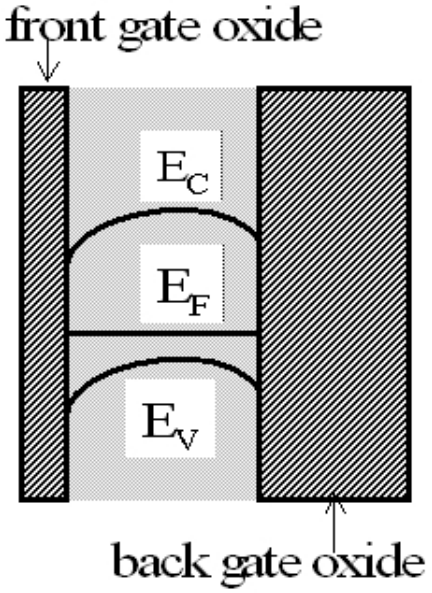

Fig. 3.2: Schematic energy band diagram of a fully depleted SOI NMOSFET when the front and back gates are biased in inversion.

3.3 Threshold Voltage of a FDSOI Device

The threshold voltage V_T of a fully depleted enhancement mode n-channel SOI device can be obtained by solving the Poisson's equation (eqn. (3.2)) using the depletion approximation [60].

$$\frac{d^2\phi}{dx^2} = \frac{qN_A}{\varepsilon_0\varepsilon_{si}} \tag{3.2}$$

Integrating eqn. (3.2) twice yields the potential as a function of depth in silicon film [61], and is given as

$$\phi(x) = \frac{qN_A}{2\varepsilon_0\varepsilon_{si}}x^2 + \left(\frac{\phi_{s2}-\phi_{s1}}{t_{si}} - \frac{qN_A t_{si}}{2\varepsilon_0\varepsilon_{si}}\right)x + \phi_{s1} \tag{3.3}$$

where ϕ_{s1} and ϕ_{s2} are potentials at the front and back silicon-oxide interfaces and N_A is the uniform substrate doping concentration. The electric field in the silicon film is given as

$$E(x) = -\frac{qN_A}{\varepsilon_0\varepsilon_{si}}x - \left(\frac{\phi_{s2}-\phi_{s1}}{t_{si}} - \frac{qN_A t_{si}}{2\varepsilon_0\varepsilon_{si}}\right) \tag{3.4}$$

The front surface electric field, E_{s1}, at x = 0 can be calculated from eqn. (3.4) as

$$E_{s1} = -\left(\frac{\phi_{s2}-\phi_{s1}}{t_{si}} - \frac{qN_A t_{si}}{2\varepsilon_0\varepsilon_{si}}\right) \tag{3.5}$$

Applying the Gauss theorem at the front interface, the potential drop across the front gate oxide ϕ_{ox1} is given as,

$$\phi_{ox1} = \frac{\varepsilon_0\varepsilon_{si}E_{s1} - Q_{ox1} - Q_{inv1}}{C_{ox1}} \tag{3.6}$$

where Q_{ox1} is the fixed oxide charge density at the front oxide interface, Q_{inv1} is the front channel inversion charge, and C_{ox1} is the front gate oxide capacitance. Similarly for the back interface,

applying Gauss theorem and using eqn. (3.5), the potential drop across the buried oxide ϕ_{ox2}, can be obtained as

$$\phi_{ox2} = -\frac{\varepsilon_0 \varepsilon_{si} E_{s1} - qN_A t_{si} + Q_{ox1} + Q_{inv1}}{C_{ox1}} \tag{3.7}$$

where Q_{ox2} is the fixed oxide charge density at the back oxide and Q_{s2} is the charge possible at the back interface in inversion ($Q_{s2} < 0$) or accumulation ($Q_{s2} > 0$). The front and back gate voltages are given as

$$at\ front\ gate \qquad V_{G1} = \phi_{s1} + \phi_{ox1} + \phi_{ms1} \tag{3.8a}$$

$$at\ back\ gate \qquad V_{G2} = \phi_{s2} + \phi_{ox2} + \phi_{ms2} \tag{3.8b}$$

where ϕ_{ms1} and ϕ_{ms2} are the front and back gate the work function differences respectively. The gate voltages can be obtained by combining eqns. (3.5) - (3.8) as

$$V_{G1} = \phi_{ms1} - \frac{Q_{ox1}}{C_{ox1}} + \left(1 + \frac{C_{si}}{C_{ox1}}\right)\phi_{s1} - \frac{C_{si}}{C_{ox1}}\phi_{s2} - \frac{\frac{1}{2}Q_{depl} + Q_{inv1}}{C_{ox1}} \tag{3.9a}$$

$$V_{G2} = \phi_{ms2} - \frac{Q_{ox2}}{C_{ox2}} - \frac{C_{si}}{C_{ox2}}\phi_{s1} + \left(1 + \frac{C_{si}}{C_{ox2}}\right)\phi_{s2} - \frac{\frac{1}{2}Q_{depl} + Q_{s2}}{C_{ox2}} \tag{3.9b}$$

Equations (3.9a) and (3.9b) are the relationships which describe the charge coupling between the front and back gates of a FDSOI MOSFET. Combing eqns. (3.9a) and (3.9b) will give the front gate threshold voltage as a function of back gate bias. The effect of front gate bias voltage and the back gate bias voltage on the substrate potential distribution is illustrated in fig. 3.3.

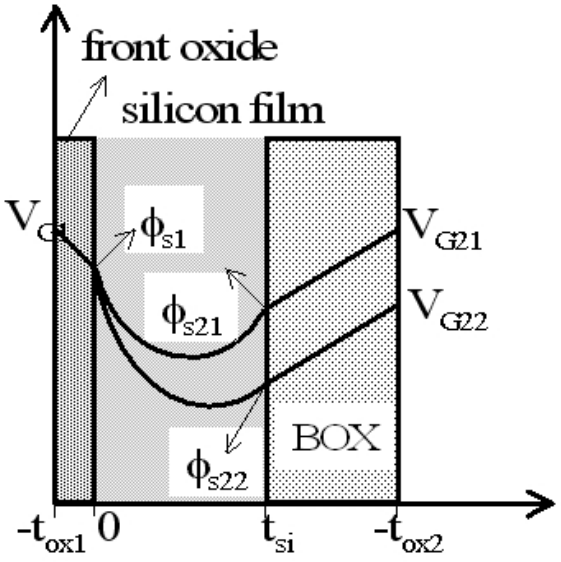

Fig. 3.3: Schematic illustration of potential distribution in the substrate of a fully depleted SOI MOSFET as a function of back gate bias while the front gate bias is held constant.

The fig. 3.3 illustrates the dependency of potential distribution over the substrate when the back gate bias is changed, while the front gate bias is held constant. It is noticeable that the minimum of the potential distribution shifts towards the front gate when the back gate bias voltage is decreased. From the front gate oxide to the minimum of substrate potential, the front gate voltage controls the

depletion region. After the minimum, the back gate controls the depletion region in FDSOI devices.

The threshold voltage of a FDSOI MOSFET when the back interface is depleted can be evaluated as

$$V_{T1,depl2} = V_{T1,acc2} - \frac{C_{si}C_{ox2}}{C_{ox1}\big(C_{si}+C_{ox2}\big)}\big(V_{G2} - V_{G2,acc}\big) \tag{3.10}$$

where $V_{T1,acc2}$ is the threshold voltage of the front surface when the back surface is accumulated and $V_{G2,acc}$ is the voltage for which the back interface reaches accumulation, and are given as

$$V_{T1,acc2} = \phi_{ms1} - \frac{Q_{ox1}}{C_{ox1}} + \left(1 + \frac{C_{si}}{C_{ox1}}\right) 2\phi_f - \frac{Q_{depl}}{2C_{ox1}} \tag{3.11a}$$

$$V_{G2,acc} = \phi_{ms2} - \frac{Q_{ox2}}{C_{ox2}} - \frac{C_{si}}{C_{ox2}} 2\phi_f - \frac{Q_{depl}}{2C_{ox2}} \tag{3.11b}$$

3.3.1 Body Effect

In a FDSOI MOSFET, the variation of threshold voltage with respect to back gate voltage can be obtained by taking the first derivative of eqn. (3.10) with respect to V_{G2}. Thus,

$$\frac{dV_{T1,depl2}}{V_{G2}} = -\frac{C_{si}C_{ox2}}{C_{ox1}\big(C_{si}+C_{ox2}\big)} \equiv -\delta \tag{3.12}$$

The body effect coefficient can be now defined as

$$n = 1 + \delta = 1 + \frac{C_{si}C_{ox2}}{C_{ox1}\big(C_{si}+C_{ox2}\big)} \tag{3.13}$$

In FD SOI devices, $C_{si} \gg C_{ox2}$ and $C_{ox1} \gg C_{ox2}$. Thus very small value δ makes the body coefficient $n \rightarrow 1$.

3.4 FDSOI Device Characteristics

In this section, the current-voltage characteristics (I-V characteristics) of a FD n-channel SOI device when the back gate is depleted will be discussed. Complex biasing of a FDSOI leads to complex device characteristics.

3.4.1 Drain Characteristics

The current voltage characteristics of a FDSOI device were derived by using the GCA [62]. The model assumes constant mobility throughout the channel region, uniform doping of the silicon film in the channel region and negligible diffusion currents. When the back interface is depleted from the source to drain end, the drain current can be obtained as,

$$I_{DS,depl2} = \frac{W}{L}\mu_n C_{ox1}\left(\big(V_{GS1} - V_{T1,depl2}\big)V_{DS} - \left(1 + \frac{C_{si}C_{ox2}}{C_{ox1}\big(C_{si}+C_{ox2}\big)}\right)\frac{V_{DS}^2}{2}\right) \tag{3.14}$$

The saturation drain voltage can be calculated as

$$V_{DSat,depl2} = \frac{V_{GS1} - V_{T1,depl2}}{1 + \frac{C_{si}C_{ox2}}{C_{ox1}\left(C_{si}+C_{ox2}\right)}} \tag{3.15}$$

and saturation drain current can be calculated as

$$I_{DSat,depl2} = \frac{1}{2}\frac{W}{L}\frac{\mu_n C_{ox1}}{1+\frac{C_{si}C_{ox2}}{C_{ox1}\left(C_{si}+C_{ox2}\right)}}\left(V_{GS1}-V_{T1,depl2}\right)^2 \tag{3.16a}$$

$$I_{DSat,depl2} = \frac{1}{2}\frac{W}{L}\frac{\mu_n C_{ox1}}{n}\left(V_{G1}-V_{T1,depl2}\right)^2 \tag{3.16b}$$

Depending upon the source bias, the back gate can be accumulated or depleted at the source end. Various combinations of front and back biases result in different drain current dependencies. This is discussed elsewhere [60].

3.4.2 Subthreshold Slope

The dependency of the surface potential of the front interface with front and back gate biases is established in eqn. (3.9a) and eqn. (3.9b). Eliminating ϕ_{s2} between the two equations and expressing ϕ_{s1} as a function of front and back gate voltages will result in

$$\begin{aligned}\phi_{s1}\left(\left(1+\frac{C_{si}}{C_{ox1}}\right)\frac{C_{ox1}}{C_{si}}\left(1+\frac{C_{si}}{C_{ox1}}\right)\right) = \\ V_{G2}-\phi_{ms2}+\frac{Q_{ox2}}{C_{ox2}}-\left(\frac{Q_{depl}}{2C_{ox1}}+\phi_{ms1}-\frac{Q_{ox1}}{C_{ox1}}-V_{G1}\right)\frac{C_{ox1}}{C_{si1}}\left(1+\frac{C_{si}}{C_{ox2}}\right)+\frac{Q_{depl}}{2C_{ox2}}\end{aligned} \tag{3.17}$$

The expression for subthreshold current is the same as in eqn. (2.53). From eqn. (2.54), eqn. (2.53) and eqn. (3.17), one can calculate the subthreshold slope as:

$$S = \frac{kT}{q}\left[1+\frac{1}{C_{ox1}}\left(\frac{C_{si}C_{ox2}}{C_{si}+C_{ox2}}\right)\right]\ln(10) \tag{3.18a}$$

$$S = \frac{kT}{q}n\ln(10) \tag{3.18b}$$

In a FDSOI device, it is generally $C_{ox2} \ll C_{ox1}$ and $C_{ox2} \ll C_{si}$. So the subthreshold slope is near to its ideal value of 60 mV/decade.

3.4.3 A.C Characteristics

The low frequency and high frequency equivalent small signal circuits of a FD SOI MOSFET are the same as shown in fig. 2.21. The same analysis for small signal circuits as explained in section 2.5.2 still stands for a first order approximation.

3.4.3.1 Transconductance

The transconductance of a FDSOI device can be obtained from eqn. (2.58b) and (3.16) as

$$g_m = \frac{\mu_n C_{ox1}}{n}\frac{W}{L}\left(V_{GS1}-V_{T,depl2}\right) \tag{3.19}$$

3.4.3.2 Cutoff Frequency

The cutoff frequency of a FDSOI device can be calculated as

$$f_T = \frac{g_m}{2\pi C_{ox1}} \tag{3.20}$$

3.5 Short Channel Effects

The short channel properties in FDSOI devices were improved when compared to a bulk device, as there is better control over depletion charge in the case of SOI devices [63]. The threshold voltage roll-off is low when compared to the bulk devices [64]. The other short channel effect DIBL is very low when compared to the DIBL of a bulk device. The short channel effects can be further minimized by heavily doping the top of the substrate under BOX [65].

If the device characteristics of a bulk CMOS device and SOI CMOS device are compared, then the device characteristics also depend upon the body factor "n". The body factor is less in the case of a FD SOI device (eqn. (3.13)), and worse in the case of a PD SOI device. If one compares the body factor values for a FDSOI MOSFET (n_{FDSOI}), PDSOI MOSFET (n_{PDSOI}) and a bulk MOSFET (n_{bulk}) then:

$$n_{FDSOI} < n_{bulk} < n_{PDSOI} \tag{3.21}$$

The inverse dependency of body factor results in better device performance in terms of drain current, transconductance and cutoff frequency and small subthreshold slope values in FD SOI devices when compared to the bulk CMOS devices.

3.6 The FINFET

When the devices are scaled down, complex doping profiles are required. These degrade the device performance. FinFET is a novel modification of SOI MOSFET, in which the channel is surrounded by a gate on three sides as in fig. 3.4 [66],[67]. The fin is a narrow channel of silicon patterned on SOI wafer. The gate wraps fin on the three faces. L is the channel length of the device, t_{si} represents the channel width and h_{si} is the height of the fin. The top insulator is generally thicker than the

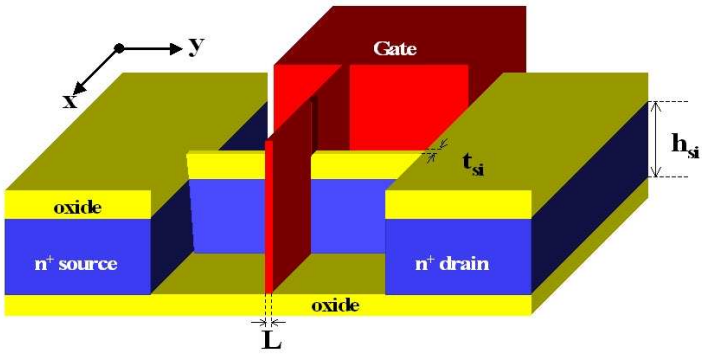

Fig. 3.4: Schematic diagram of a FINFET.

side insulators, therefore the device effectively has two channels. The FINFET is one of the most popular double gate devices because the two gates are self aligned to the source and drain and spacer technology can be used to pattern ultra-thin fins.

3.7 Conclusions

The SOI CMOS devices are a novel variation of bulk CMOS devices. The SOI devices are of two types, namely PD SOI devices and FD SOI devices depending upon silicon film thickness. The device

characteristics of FD SOI were talked about in this chapter. In the next chapter, the fabrication and simulations of bulk CMOS devices and FDSOI devices will be discussed. The simulation structures are also explained.

4

Device Fabrications and Simulations

4.1 Introduction

In this section, the basic device fabrication of bulk CMOS devices and FD SOI CMOS devices will be discussed. These device fabrication steps will be helpful in later parts for the process simulations, which is part of this work.

4.2 Bulk CMOS Device Fabrication

In dual work function gate technologies, to fabricate CMOS devices, a p^--type $< 100 >$ silicon substrate with a substrate resistivity of $2\,\Omega$-cm was considered. To fabricate a p-channel MOSFET, a high energy high dose arsenic implant was performed to produce a n-well by converting the substrate locally. In order to fabricate a n-channel MOSFET, a p-well was formed with a p-type implant. The dual well technologies allow separate optimization of the NMOSFET and PMOSFET. An inert ambient temperature drive-in was performed to activate and to diffuse the dopant atoms into silicon substrate to form n-well and p-well in the silicon substrate. The NMOSFET is fabricated in a p-well and n-well is used to fabricate a PMOSFET. Any implantation steps, for example, V_T adjust implantation, are done through the sacrificial oxide layer. A LOCOS (LOCal Oxidation of Silicon) isolation scheme or STI (Shallow Trench Isolation) are practiced in order to isolate the active areas of the devices. After the completion of LOCOS or STI isolation, the resulting structure is shown in fig. 4.1 and fig. 4.2. It is noticeable from the LOCOS and STI isolation schemes, that LOCOS isolation needs more lateral space and the topology is complicated when compared to STI isolation. In order to gain more active area in a device, STI isolation is preferred over LOCOS isolation in small dimension devices. After the isolation steps, the process steps to form a device are almost identical in both isolation schemes. To fabricate a device in the n-well, the p-well is masked and vice versa. So to make it simpler, only the processing steps of a NMOSFET are briefly discussed. The gate oxide is grown and the poly silicon gate is deposited and patterned. In identical long channel devices, high energy (20-50 keV) gate and source/drain implants were combined to dope the poly silicon gate and to form source/drain regions. However, in short channel devices, the gate implant energy differs from self aligned source/drain implants, due to the source/drain junction depth limitations,. Contact formation and passivation of the device completes the device fabrication. The important steps after

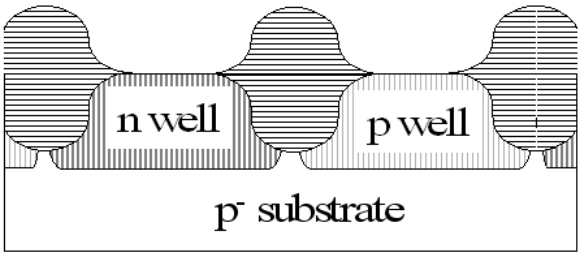

Fig. 4.1: Illustration of a p^- doped substrate after LOCOS isolation to process CMOS devices.

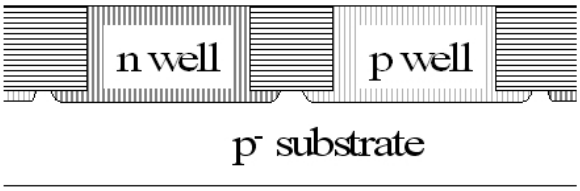

Fig. 4.2: Illustration of a p^- doped substrate after STI isolation to process CMOS devices.

isolation are shown in fig. 4.3 [68].

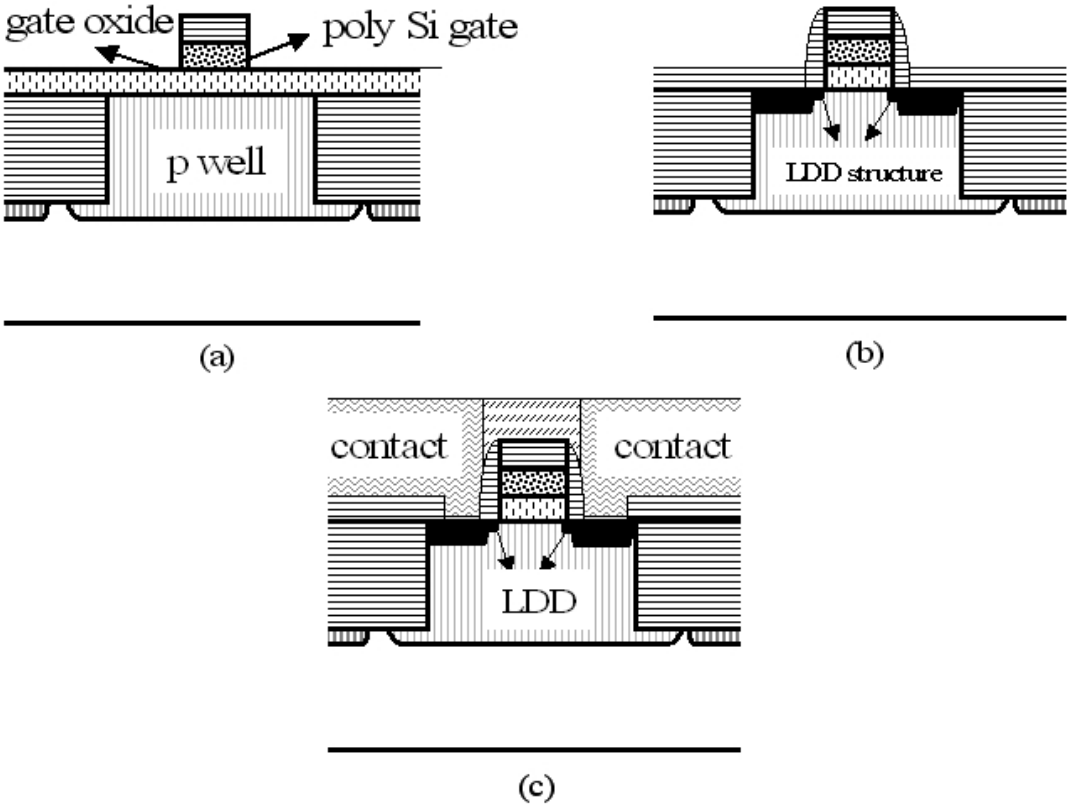

Fig. 4.3: Illustration of the different process steps in a STI isolated NMOSFET (a) gate oxide deposition and poly gate patterning (b) source/drain formation with LDD extensions and (c) fully processed device structure after contact formation.

4.3 SOI Device Fabrication

The starting material for SOI device fabrication is a SOI wafer, fabricated by using some of the existing techniques like, SIMOX (separation by implanted oxygen) [69], Smart-Cut® [70] or eltran® (epitaxial layer transfer) [71]. The subsequent processing steps are almost identical to that of a bulk

Bulk CMOS	FDSOI CMOS
well preparation	-
nitride deposition	nitride deposition
active area lithography	active area lithography
device isolation	device isolation
p-channel lithography	-
gate oxide growth	date oxide growth
p-channel blanket V_T implant	p-channel blanket V_T implant
n-channel blanket V_T lithography	n-channel blanket V_T lithography
n-channel anti-punch-through implant	-
poly deposition and doping	poly deposition and doping
gate lithography and etch	gate lithography and etch
source/drain formation	source/drain formation
oxide deposition	oxide deposition
contact formation	contact formation
anneal	anneal

Table 4.1: Comparison between process flow of bulk and FDSOI CMOS device fabrication.

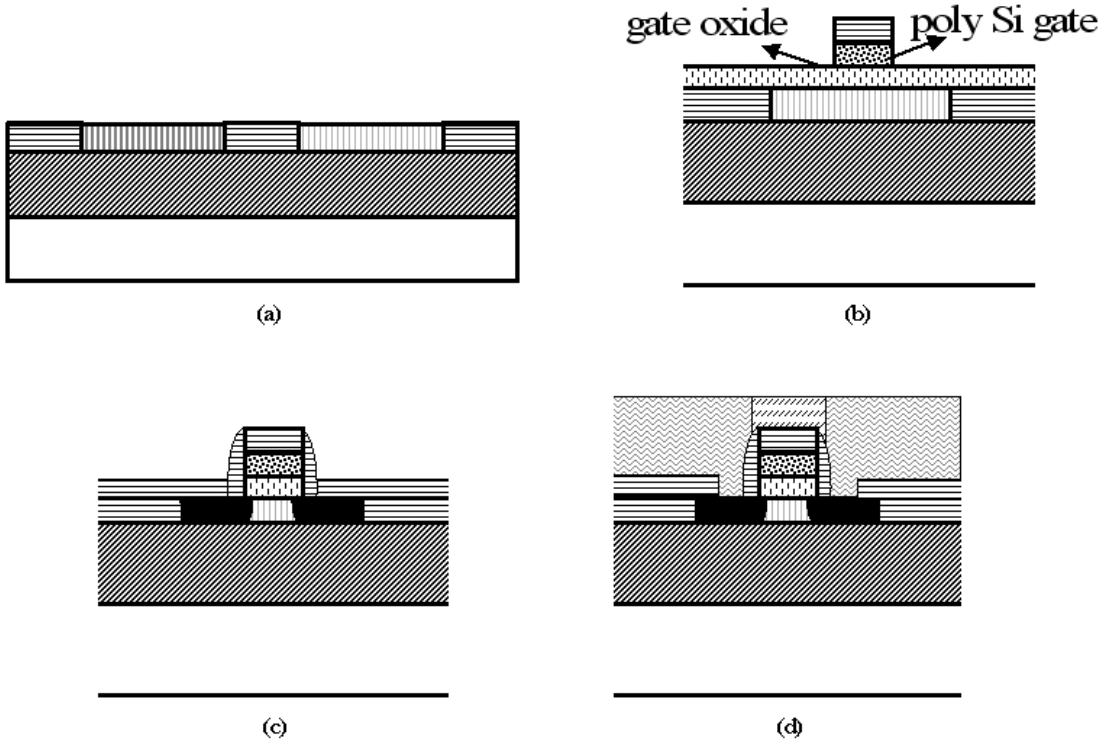

Fig. 4.4: Illustration of various processing steps of a FDSOI device (a) isolation by STI scheme (b) gate oxide deposition and poly gate patterning (c) source/drain formation and (d) complete device structure after the source/drain contact formation.

CMOS process. However SOI needs fewer processing steps when compared to bulk CMOS. Table 4.1 lists important processing steps in a bulk CMOS and FD SOI device process [60]. The FDSOI

process flow including STI device isolation is shown in fig. 4.4.

4.4 Description of Simulator

In this section the working principle of the numerical process and device simulators, namely T-SUPREM-4® and MEDICI® are briefly discussed.

4.4.1 Process Simulations

The simulator used for process simulations is the TSUPREM-4. A complete processing routine can be simulated similar to the processing steps used in the manufacturing of silicon integrated circuits and discrete devices. TSUPREM-4 simulates the incorporation and redistribution of impurities in a two-dimensional device cross-section perpendicular to the surface of the silicon wafer. The output information provided by the program includes:

- various layers of materials in the structure and the boundaries between various materials
- distribution of impurities within each layer
- stresses produced by oxidation, thermal cycling, or film deposition

A TSUPREM-4 simulated structure consists of a number of regions, and can be assigned to an individual material. Each material can be doped with impurities. The materials available in TSUPREM-4 are single crystal silicon, poly-crystalline silicon, silicon dioxide, silicon nitride, silicon oxynitride, titanium, titanium silicide, tungsten, tungsten silicide, photo-resist and aluminum. Apart from these pre-defined materials, other required novel materials can be specified in the simulator by the user. Example of common impurities are: boron, phosphorus, arsenic, antimony etc. TSUPREM-4 also simulates the distribution of point defects (interstitials and vacancies) in silicon layers and their effects on the diffusion of impurities.

The types of processing steps modeled by the current version of the program include:

- oxidation of silicon
- ion implantation
- inert ambient drive-in
- silicon and poly-silicon oxidation and silicidation
- epitaxial growth
- low temperature deposition and etching of various materials

Simulation Structure:

TSUPREM-4 simulator can process and simulate a two-dimensional cross-section of a semiconductor structure. Here, the x-coordinate represents the distance parallel to the surface of the wafer, and the y-coordinate corresponds to the depth into the wafer. In plots of the structure, the coordinate increases from left to right, and y increases from the bottom to the top. In specialized applications, the coordinate also lies parallel to the surface of the wafer, giving a simulation space in the plane of the wafer surface. The coordinate system is fixed relative to the initial structure,

thus fixing the bottom of the substrate. The initial structure is user-defined and is defined as a rectangular region of arbitrary width and depth. By default, the top of the structure is exposed, and reflecting boundary conditions are applied to the sides. Deposition, etching, impurity pre-deposition, oxidation, silicidation, reflow, and out-diffusion occur at exposed surfaces, while photolithographic exposure and ion implantation usually occur normal to the surface.

The simulated structure can consist of one to forty regions of arbitrary shape and dimensions. Each region consists of a single material. By definition, adjacent regions (i.e., regions that meet along an edge) contain different materials. The same material can be present in multiple (non-adjacent) regions. The continuous physical processes which are modeled in TSUPREM-4 are approximated numerically using finite difference (for diffusion) and finite element (for oxide flow) solution techniques. Each region of the structure is divided into a mesh of non-overlapping triangular elements. There can be up to 80,000 triangles in the entire TSUPREM-4 mesh structure. Solution values are calculated at the mesh nodes at the corners of the triangular elements. At points where two or more materials meet, there are multiple solution values (multiple nodes), one for each material at the meeting point. On an exposed boundary, there is also an extra node at each point, which represents concentrations in the ambient gas. The total number of nodes in a structure is calculated by adding the number of mesh points in each material, to the number of mesh points along exposed boundaries. To start a process simulation, first a grid structure must be defined. One can define an initial grid structure by explicitly specifying the locations and spacing of grid lines, or automatically generating a grid given the width and (optionally) the locations of mask edges. Once an initial grid has been defined, it is adjusted automatically as various process steps are simulated. The initial grid applies to the structure, not to the space containing the structure. Thus, the processing steps that change the device structure must change the mesh structure as well. The processing steps that change the grid are deposition, epitaxy, etching, photo-resist development, oxidation, and silicidation. In addition, if adaptive gridding is enabled, the grid may be modified during ion implantation and diffusion. The process simulator can import mask structure form a user defined file and thus the processing steps can be simulated similar to a real process.

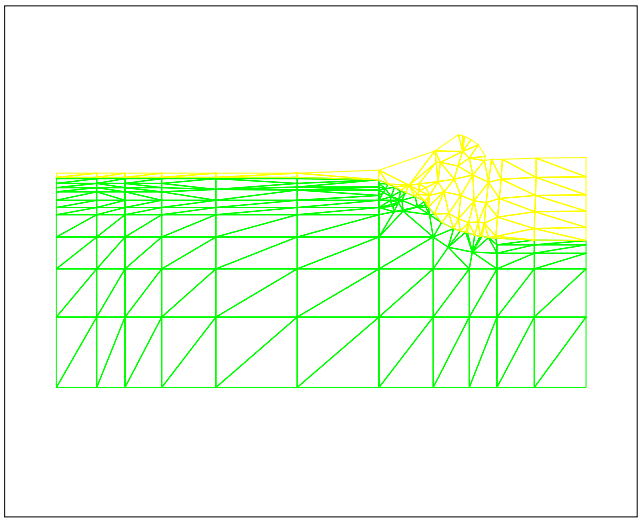

Fig. 4.5: Illustration of grid generated in simulating LOCOS isolation to process simulate a CMOS devices.

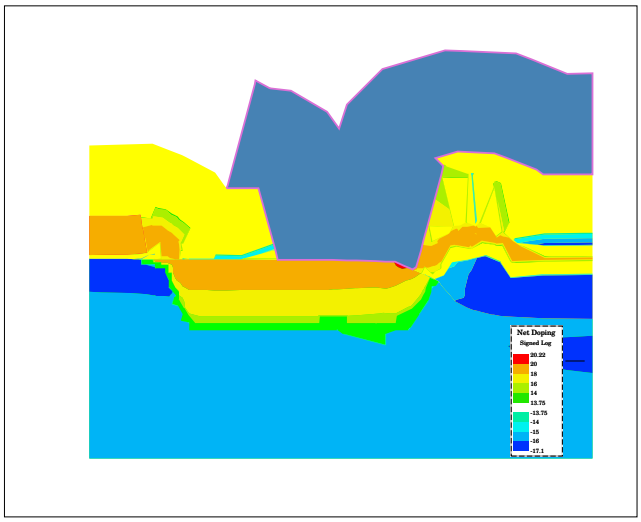

Fig. 4.6: A structure of process simulated half CMOS device, showing the doping distribution.

The simulations are initiated by defining a wafer of desired orientation and substrate doping type and concentration. Then the preliminary grid structure was specified. Isolation, p-well and

n-well implantation and a drive-in were performed. Gate oxide deposition/growth, gate formation followed by source and drain implantation define the active areas. The source/drain anneals followed by a metallization finishes the device processing with relative mask definitions at each step. With appropriate process steps and mask levels, a complete CMOS device can be process simulated. While process simulating the devices, due to the symmetry of the MOSFET along the plane passing through the center of channel, to save computational efforts and time, it is a general practice to simulate one half of the device as shown in fig. 4.5 and fig. 4.6. The remaining half is reflected accordingly to obtain the full structure of the device. A simulated NMOSFET showing the complete mesh, junctions and different material regions is shown in fig. 4.7 and fig. 4.8. The mesh generated while process simulating a SOI structure is shown in fig. 4.9 and the structure of a process simulated FD SOI device is shown in fig. 4.10.

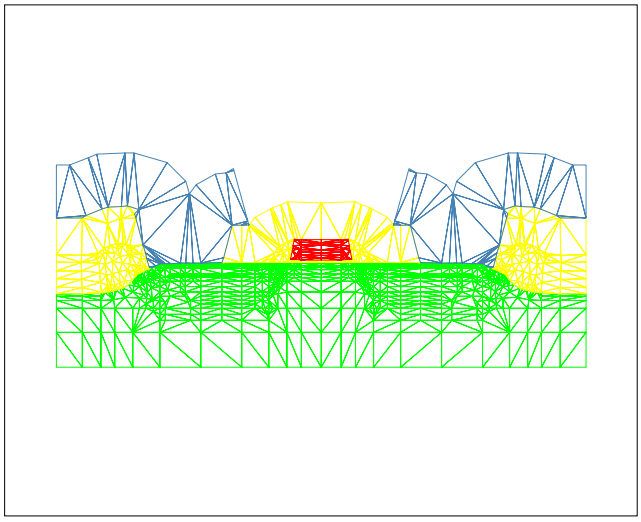

Fig. 4.7: Complete grid of a CMOS device after process simulations.

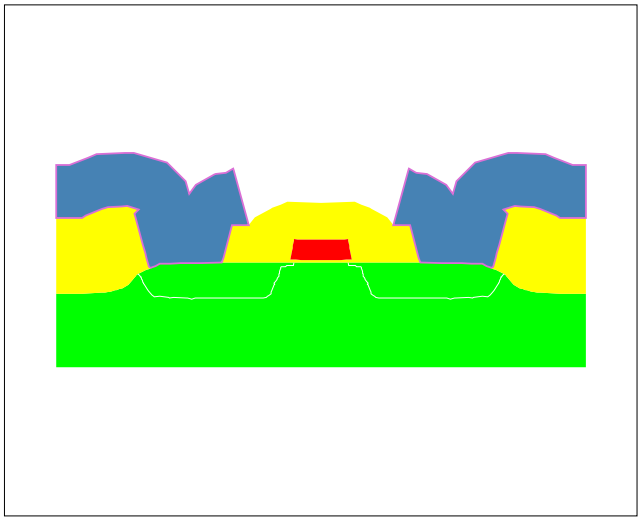

Fig. 4.8: Complete structure of fully process simulated CMOS device.

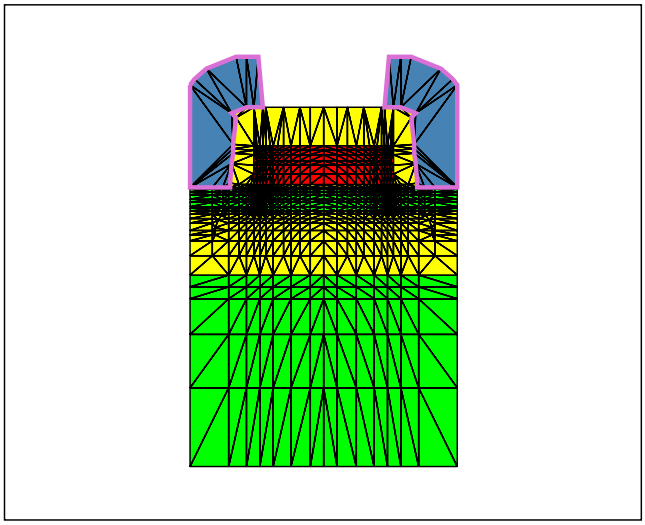

Fig. 4.9: Illustration of grid generated while simulating a FS SOI CMOS device.

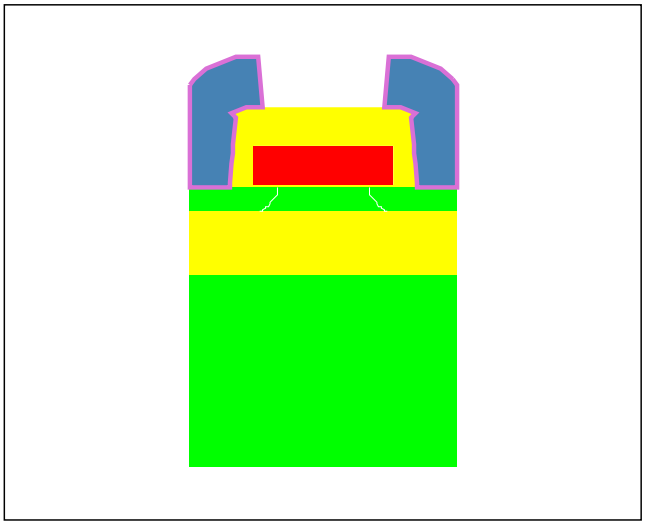

Fig. 4.10: Structure of process simulated FD SOI CMOS device.

The process simulated structure can be then exported into the device simulator MEDICI. The exported process simulated profile consists of dopant type, doping concentration, gate oxide thick-

ness, information about various junctions and regions. This data can be used to obtain the device characteristics at arbitrary biasing conditions. A more detailed description of the simulator can be found in the TSUPREM-4 user manual [72].

The process simulator was calibrated and adjusted to available industrial CMOS hardware by simulating a full process sequence of CMOS devices.

4.4.2 Device Simulations

Medici is a device simulation program that can be used to simulate the behavior of MOSFETs, bipolar transistors and various other semiconductor devices. It models the two-dimensional distributions of potential and carrier concentrations in a device. The program can be used to predict the electrical characteristics of semiconductor devices for arbitrary bias conditions. The device characteristics are simulated by either using a pre-process simulated file, which can be imported from a process simulator such as TSUPREM-4, or by defining a structure in Medici itself. In addition, Medici can be used to study devices under transient operating conditions. In the era of sub micron devices, Medici simulates the behavior of deep sub-micron effects by providing the ability to solve the electron and hole energy balance equations self-consistently with the other device equations. Effects such as carrier heating and velocity overshoot are accounted for in Medici, and their influence on device behavior can be analyzed. The basic equations which are solved by Medici are the Poisson's equation (eqn. (4.1)) and the electron and hole current continuity equations (eqn. (4.2a) and eqn. (4.2b)).

$$\varepsilon_r \varepsilon_0 \nabla^2 \Phi = -q\big(p - n + N_D^+ - N_A^-\big) - \rho_S \tag{4.1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\vec{\nabla} \cdot \vec{J_n} - U_n = F_n\big(\Phi, n, p\big) \tag{4.2a}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\vec{\nabla} \cdot \vec{J_p} - U_p = F_p\big(\Phi, n, p\big) \tag{4.2b}$$

where Φ is the Fermi potential and N_D^+ and N_A^- are the ionized impurity concentrations and ρ_S is the surface charge density that may be present due to fixed charge in insulating materials or charged interface states while, U_n and U_p are the net electron and hole recombination components. From Boltzmann transport theory, the electron current density $\vec{J_n}$ and hole current density $\vec{J_p}$ in eqns. (4.2a) and (4.2b) can be written as functions of the carrier concentrations and the Fermi potentials for electrons and holes, ϕ_n and ϕ_p as

$$\vec{J_n} = q\mu_n n\vec{\phi_n} \tag{4.3a}$$

$$\vec{J_p} = q\mu_p p\vec{\phi_p} \tag{4.3b}$$

Alternatively, $\vec{J_n}$ and $\vec{J_p}$ can be written as functions of ϕ, n, and p, consisting of drift and diffusion components

$$\vec{J_n} = q\mu_n n\vec{E_n} + qD_n\vec{\nabla}n \tag{4.4a}$$

$$\vec{J_p} = q\mu_p p\vec{E_p} - qD_p\vec{\nabla}p \tag{4.4b}$$

with $\vec{E_n} = \vec{E_p} = \vec{E}$ = -$\vec{\nabla}\phi$. Here $\vec{E_n}$ is the electric field distribution due to electrons and $\vec{E_p}$ is the electric field due to holes. From the above equations ((4.1) to (4.4)), the carrier distribution, charge density distribution, electric field intensity, potential and thus the current in the device can be

calculated at the desired biasing conditions. The most important parameter in the MOSFET device characteristics, the mobility of carriers can be incorporated and different mobility models, which consider the effects and dependency of mobility on channel doping, electric fields and scattering mechanisms can be used depending upon the requirements. Examples of the simulated electrical field distribution and potential distributions are shown in fig. 4.11 and fig. 4.12 respectively. A more detailed description about the simulator can be found in the MEDICI user manual [73].

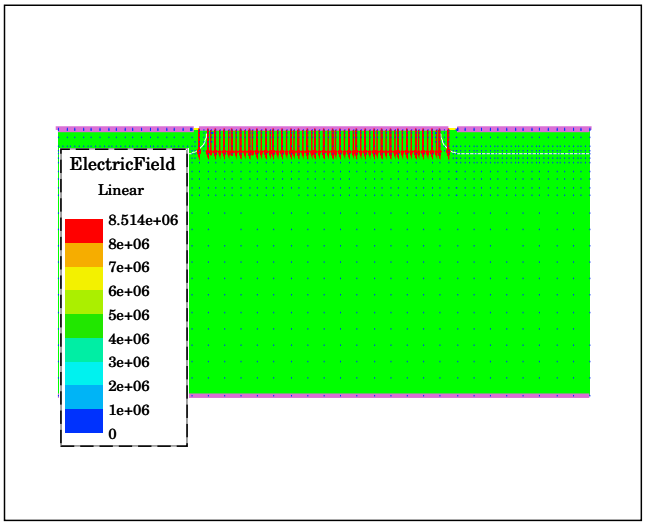

Fig. 4.11: Illustration of electric field distribution in a MOSFET simulated by using MEDICI.

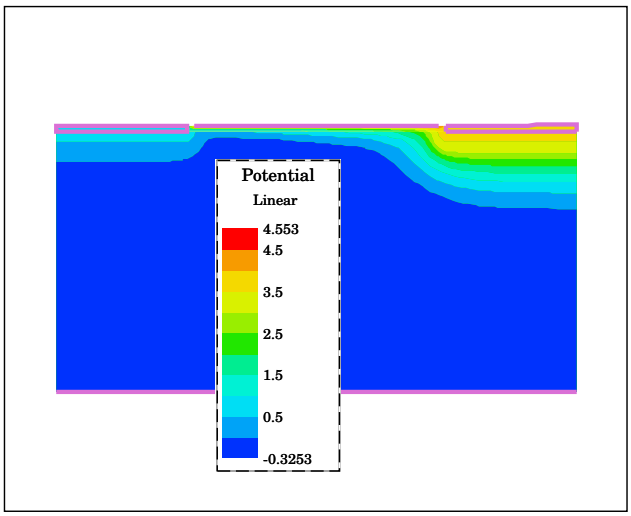

Fig. 4.12: Illustration of potential distribution in a MOSFET simulated by using MEDICI.

4.5 Simulator Optimization

The device simulator was optimized according to the flowchart illustrated in fig. 4.13. Industry standard hardware was characterized by measuring drain current characteristics and subthreshold characteristics [74], as discussed in section 2.5.3. According to industry standard protocol, the process simulator is used to simulate the process. The process simulated MOSFET structures are then exported into the device simulator to determine the threshold voltage and compared with the measured values. If required, fine adjustments in the threshold voltage were done by modifying the process parameters like channel doping, furnace process for dopant activation. Again in regard to the adjusted process parameters, the threshold voltage is once again compared with the measured value. This process is iterated until a good comparison was obtained between the measurements and simulations. After being adjusting for the threshold voltage, the process simulated structures were used to simulate the device I-V characteristics and are compared with the simulated I-V characteristics. Different mobility models which account for various degradation mechanisms, as discussed in 2.5.1.2 were chosen to simulate the device characteristics. The simulated device characteristics were then compared with the measured characteristics. To adjust to the deviations in simulated device characteristics, the mobility parameters were adjusted and the threshold voltage consistency was checked. Threshold voltage deviations were again adjusted by process simulations and with newly selected models, device characteristics were simulated. This process is repeated until the model optimization to obtain the simulated device characteristics which were identical with the measured device characteristics. The optimized parameters were used in further simulations.

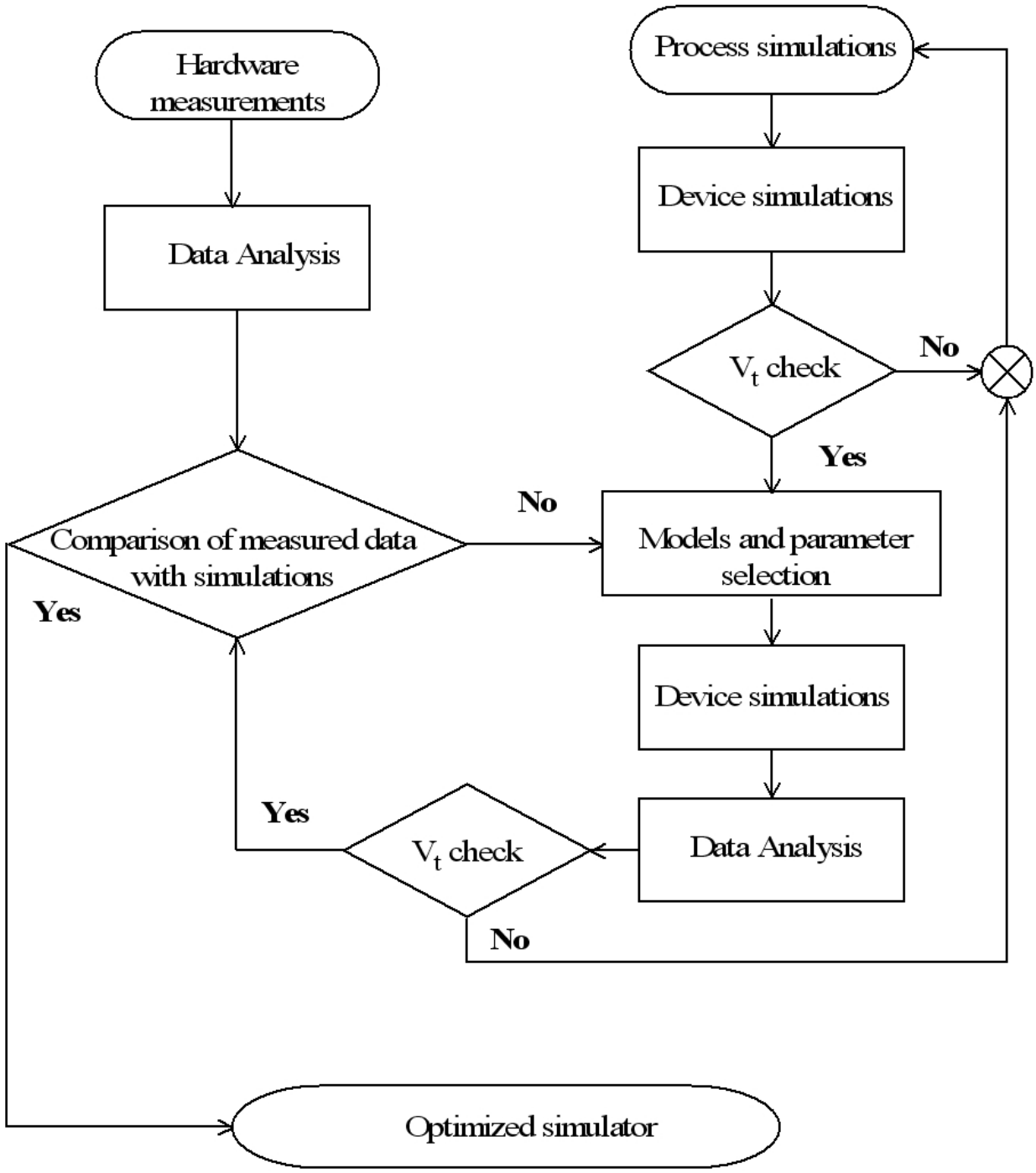

Fig. 4.13: Schematic steps followed while standardizing the simulator.

4.6 Conclusions

In this chapter, the processing sequence of bulk CMOS devices and FD SOI CMOS devices were briefly explained using the STI scheme. The process simulator and device simulator which are used to simulate the CMOS devices using STI scheme are explained briefly. The optimized process simulator and device simulator were used to obtain the device characteristics, which are explained in later chapters.

5 Gate Stack Concepts

5.1 Introduction

The gate stack in modern CMOS devices differs from the conventional gate stack. The introduction of high-k materials as a replacement to SiO_2 and non ideal gate electrode are main deviations in the gate stack in modern CMOS technologies. This chapter gives an overview of the gate stack in modern days technologies.

5.2 Advanced Gate Stacks

In sub-micron and deca nanometer devices where the channel length is less than 1 μm, the gate oxide thickness should be scaled down drastically. In deca nano meter devices, the EOT approaches a few tens of a nanometer and with 40 nm technology node, EOT should be scaled down to sub 1 nm regime [3]. Very thin gate oxides result in increased gate leakage currents and because of the process variations, the thickness variations in the gate oxide are pronounced. In addition to this, the poly gate depletion effect (PGD), as discussed in section 2.8.2.1, becomes more prominent as the gate oxide thickness decreases. As a result, the gate capacitance is no longer C_{ox} and C_{ox} reduces severely with reduction in EOT. The poly gate depletion in-turn introduces a new effect called Remote Coulomb Scattering (RCS) which is discussed in 2.8.3. The possible solutions to eliminate the poly gate depletion effect and thus to suppress the RCS are discussed in the next sections.

5.3 Depletion Free Gate Electrodes

In order to improve the performance of the highly scaled devices, elimination of the poly gate depletion and RCS is necessary. As RCS originates from the parasitic charges from poly gate depletion, the elimination of poly gate depletion means the elimination of RCS. In the following sections, the possible gate electrode architectures, which can be used for ultra thin EOT systems to eliminate the poly gate depletion and their contribution towards the device performance improvement will be discussed.

5.3.1 Metal Gate Electrodes

Metal gates provide one possible solution, and can effectively eliminate gate depletion. The gate metal should be selected in such a fashion that the energy difference between the metal fermi level and conduction band edge of the gate dielectric is high enough to prevent the charge injection. In the era of high-K dielectrics, every high-K needs at least a priori, two separate metals for gate electrode for NMOSFET and PMOSFET.

To study the effect of metal gates on device performance NMOSFETs with metal gate electrodes and poly gate electrodes with praseodymiumoxide (Pr_2O_3) as a gate dielectric were process simulated using TSUPREM-4. The simulated devices have an EOT of 1.8nm and a V_T of 0.4V. The process simulated device structures were then exported in MEDICI to simulate the drain current characteristics. The drain characteristics of metal gate NMOSFETs were compared with their poly gate counterparts as shown in fig. 5.1.

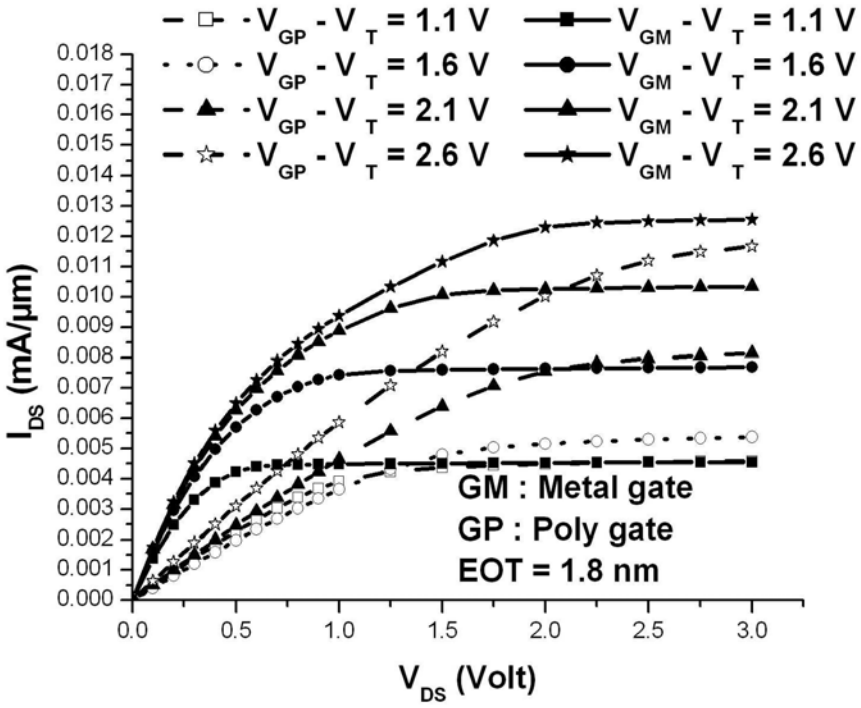

Fig. 5.1: Drain current (I_D - V_D) characteristics of a NMOSFET with a metal gate (solid lines) and highly doped poly gate (dashed lines).

A comparison between drain characteristics of metal gate MOSFETs with a highly doped poly gate MOSFETs is made and the results are shown in fig. 5.1. It is noticeable that the drain currents in a highly doped poly gate MOSFET are slightly higher at higher gate voltages but the drain current decreases after a certain increase in gate voltage when compared to its metal gate counter part. The effect of gate depletion explains the behavior of drain characteristics. As has been said earlier, all the MOSFETs have same V_T, the metal gate MOSFET and high-doped poly gate MOSFET require a high amount of implantation doses for the V_T adjustment, in order to compensate for the work function differences. Because of the high V_T implantation dose in the case of the metal gate MOSFETs, the effective mobility of the carriers decreases significantly. Therefore one observes a better drain current in the case of poly gate structures with gate depletion when compared to its counterparts

at low gate voltages. At higher gate voltages, the poly gate depletion deteriorates the drain current. Thus the advantage gained in drain current in the case of MOSFETs with poly gates but only at low gate voltages is finally over compensated by the poly gate depletion. This effect is again confirmed by a comparison of the drain characteristics of a highly doped poly silicon gate MOSFET with the metal gate MOSFET at higher gate voltages.

With many possible high-K materials, which can replace the still existing SiO_2, every high-K/ metal system needs a different study. The low melting temperature of metals means that, the high temperature post processing steps after gate deposition should be avoided. The processing of metal gates is expensive as it needs extra mask levels and replacement gate technologies, in which a dummy gate is replaced by a metal gate after the high temperature processing steps [75], [76].

The integration of metal gates architectures into the CMOS process is very critical. The processing of metal gates becomes even more complicated as the fermi level of the metal is temperature dependent due to the metal induced gap states [77]. The small variations in processing temperatures which may result in the metal work function difference, which in turn will result in a shift in flat band voltage and thus a shift in the threshold voltage of the device. Using the same metal gate material for both PMOSFET and NMOSFET can be a solution. However, using a single metal gate can lead to buried channel devices or the necessity of high dose implants to increase the doping in the channel for V_T adjustments depending upon the fermi level of the metal gate [78].

In this work, an *alternative gate doping scheme* is suggested, by which the poly gate depletion can be completely eliminated, thus improving the device performance. The next section will discuss the principle of the alternative doping scheme.

5.4 Alternative Gate Doping Scheme

In order to eliminate both effects without the need for introducing metal gate electrodes, we propose an alternative gate doping scheme to dope the poly silicon gate. In conventional devices, the gate is symmetrically doped with respect to source/drain as shown in fig. 2.31. With alternative gate

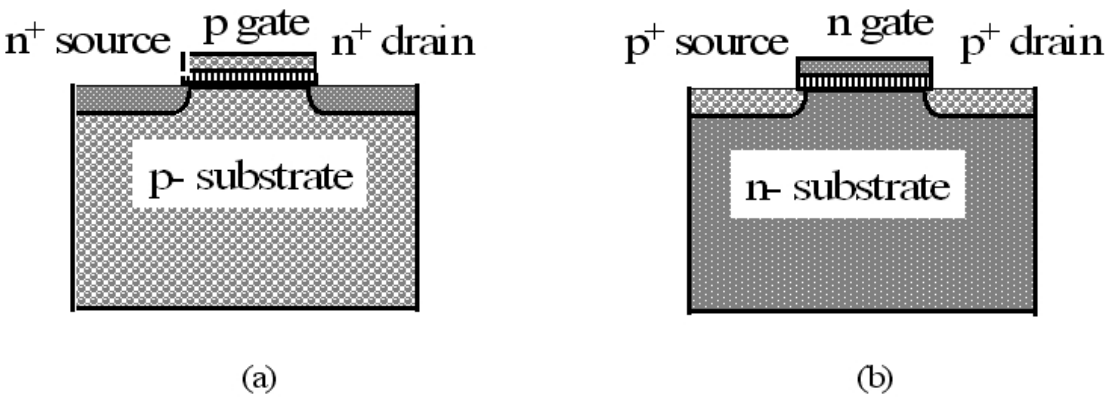

Fig. 5.2: Illustration of alternative gate doping scheme for (a) NMOSFET and (b) PMOSFET.

doping, the poly gates are inversely doped, i.e. the n^+ poly gate in the NMOSFET is replaced by a

p-type poly gate and the p^+ poly gate in the PMOSFET with a n-type poly gate as shown in fig. 5.2. When an NMOSFET is biased in inversion, a positive voltage is applied to the gate. Thus the

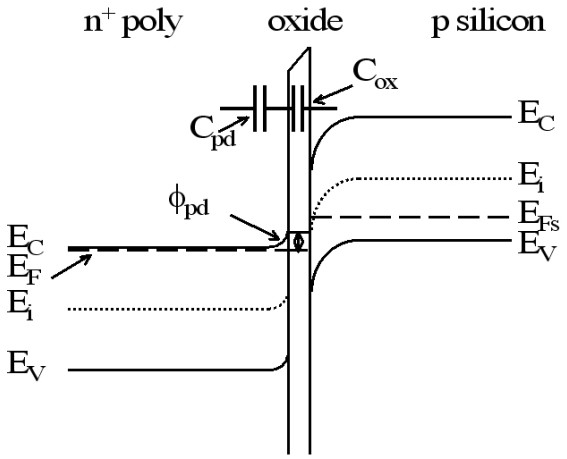

Fig. 5.3: Band diagram showing the elimination of poly gate depletion when a positive gate voltage is applied to the p poly silicon gate of a NMOSFET (PMOSC). As a result of the elimination of poly gate depletion, the poly silicon gate is driven into accumulation when the MOSFET is turned on.

p-type poly silicon gate of the device will not be driven into depletion. Similarly, for a PMOSFET, when biased in inversion, the negative voltage on the gate results in a nondepleted n-type poly silicon gate. When the device is turned on, the gate is driven into accumulation, instead of depletion. The resultant band diagram after the elimination of poly gate depletion is shown in fig. 5.3. Even though the accumulation gate charges are present at the gate electrode-gate oxide interface, the accumulation charges can follow the applied gate bias. As a result, when the MOSFET is in "ON" state, the gate capacitance is retained at its maximum value C_{ox}, as shown in fig. 5.4. In this type of gate doping scenario, due to the negative bias on the gate when the device is in "OFF", the poly silicon gate gets depleted in the "OFF" state of the transistor.

For inversely doped gates, as the gate depletion is completely eliminated when the device is turned on, RCS is also completely eliminated as there are no parasitic gate charges present in the gate electrode when the device is turned on. However, due to the work function difference between the n^+ poly silicon gate and p-poly silicon gate, the devices are buried channel devices when the devices are long channel devices. When the channel length is scaled down, due to V_T roll off, the threshold voltage of the device decreases. In order to improve the V_T of the device either a V_T adjust implant can be performed or the flat band voltage V_{FB} can be adjusted. Instead of performing a V_T adjust implant, the V_T is adjusted by adjusting the work function difference of the poly silicon gate, i.e, by using a p-type poly silicon gate in the case of a NMOSFET and by using a n-type poly gate in the case of a PMOSFET. Thus when the device is scaled down, the V_T roll off leads to a surface channel device as shown in fig. 5.5 [7].

In order to prove the concept of the alternative gate doping scheme, NMOSFETs and PMOSFETs of various channel length ranging from 200nm down to 40 nm with various EOT values ranging from 2nm down to 0.5nm were process simulated using TSUPREM-4. The process simulated profiles were then exported into MEDICI to obtain the device characteristics. In each case the gate doping type and gate doping concentration are varied to study the effect of PGD on the devices. Furthermore,

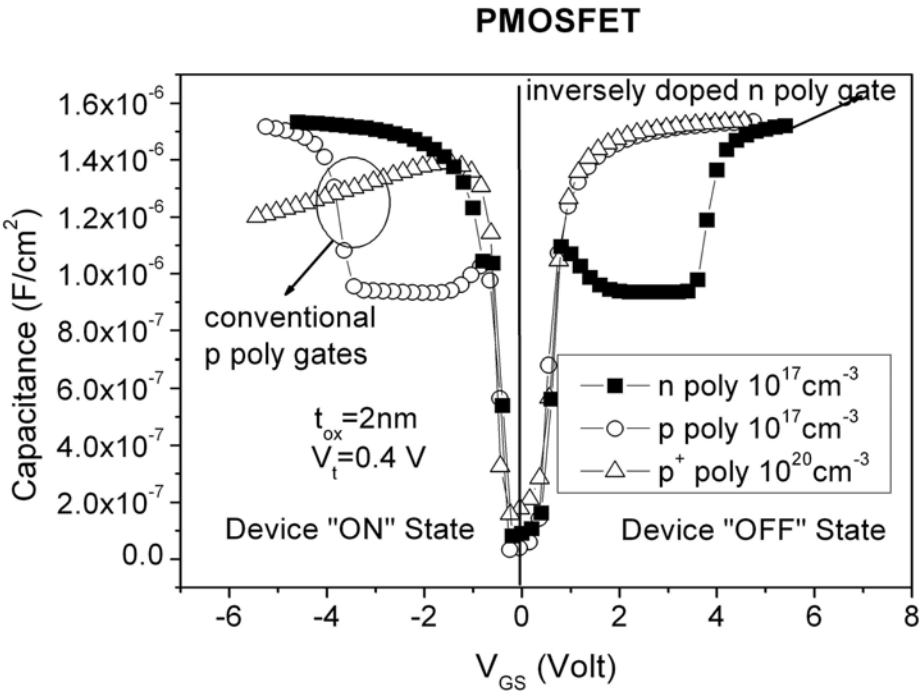

Fig. 5.4: C-V characteristics of a PMOSFET (NMOSC) when the poly silicon gate is inversely doped, showing the improvement in gate capacitance when the devices are turned on.

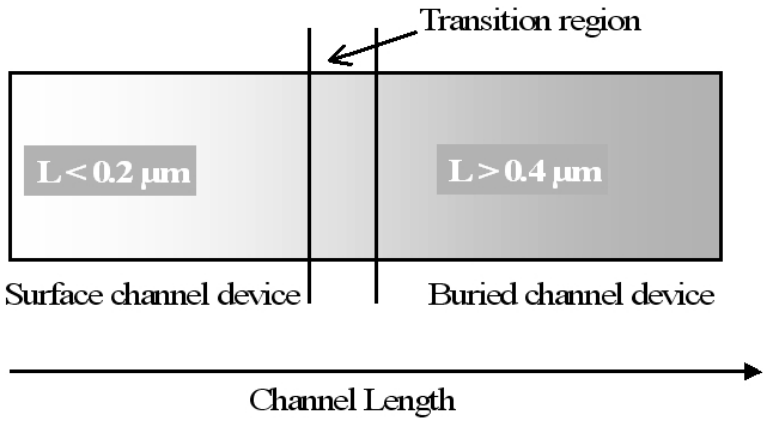

Fig. 5.5: Schematic illustration representing channel transition of a inversely doped gate MOSFET from a buried channel to a surface channel.

NMOSFETs and PMOSFETs with a metal gate were simulated to study the effect of RCS on the device performance. Similar studies were performed on FD SOI NMOSFETs and FD SOI PMOSFETs. The concept of *alternative gate doping scheme* is verified with corresponding hardware. The device simulations, hardware fabrication and measurements on alternatively doped gates are discussed in chapter 6.

5.5 Conclusions

The poly gate depletion effect and remote Coulomb scattering are two mechanisms which are unavoidable effects in modern CMOS devices. Using poly gate results in poly depletion. The highly doped poly gate which was used to decrease poly gate depletion causes remote Coulomb scattering of charge carriers in the channel. To suppress these effects, metal gates can be used. However, metal gates are difficult to fabricate. The alternative gate doping scheme which was explained in this chapter, to suppress poly gate depletion when the device is turned on thus eliminating RCS.

6 MOSFET Results and Discussion

6.1 Introduction

The alternative poly gate doping concept as explained in chapter 5 was studied extensively via simulations. The simulations were performed on NMOSFETs and PMOSFETs for both bulk and FDSOI devices. Preliminary results on the alternate gate doping concept were published in [7] prior to other research groups [79]. The concept of alternative gate doping scheme used to achieve inversely doped gate electrodes was verified with corresponding hardware. This chapter provides a brief overview and summary on some of the important results.

6.2 Device Simulations

The alternative gate doping concept was verified by means of extensive simulation studies of CMOS devices. Both PMOSFETs and NMOSFETs with channel length ranging from 200 nm down to 40 nm with an equivalent gate oxide thickness from 2.0 nm to 0.5 nm were process simulated using process simulator TSUPREM-4. The final target of process simulation is to simulate MOSFETs with an identical threshold voltage of $|0.4|$ V. The structures were later exported into the device simulator MEDICI, to study the device characteristics. The doping of the gate in the case of inversely doped devices is studied from 10^{15} dopant atoms cm^{-3} up to 10^{20} dopant atoms cm^{-3}. However, due to the high resistivity of the gate, which is due to its low doping concentration, the devices with a gate doping concentration below 10^{17} atoms cm^{-3} were not considered while the devices with a gate doping concentration 10^{17} atoms cm^{-3} and above were studied in detail. Table 6.1 gives the common device parameters which were used in simulating both conventionally doped gates and inversely doped gate MOSFETs.

When the EOT is more than 1 nm, SiO_2 is used as the gate dielectric. A transition was made from SiO_2 based gate dielectric to high-K gate dielectric material (Pr_2O_3) at an EOT of 1 nm. A comparison of the device characteristics of a PMOSFET with an EOT of 1 nm but with different gate insulators, namely SiO_2 and Pr_2O_3 is shown in fig. 6.1. The drain current characteristics show a perfect match, resulting in a smooth transition of the MOSFETs with SiO_2 as the gate dielectric to MOSFETs with Pr_2O_3 as gate dielectric. The variation of gate doping concentration

L(nm)	EOT (nm)					
	2.0 (SiO_2)	1.5 (SiO_2)	1.0 (SiO_2)	1.0 (Pr_2O_3)	0.75 (Pr_2O_3)	0.50 (Pr_2O_3)
150	×	×	×	×	×	×
100	×	×	×	×	×	×
60	×	×	×	×	×	×
40	×	×	×	×	×	×

Table 6.1: Matrix of parameters of MOSFETs used in device simulations.

and gate doping type on device performance were studied in detail. In order to facilitate the study, conventional gate NMOSFETs and PMOSFETs have a gate doping concentrations of $10^{19}cm^{-3}$ and $10^{20}cm^{-3}$ in the case of a lowly doped gate and for a highly doped gate respectively. In the case of alternatively doped devices, the gate doping is a function of channel length and equivalent oxide thickness, which is discussed in later sections (section 6.3.3). The conventional poly gates were later replaced with metal gates with a suitable work function. The replacement of conventionally doped poly gate electrodes with the metal gate electrodes makes it easier to study the effect of poly gate depletion and remote Coulomb scattering.

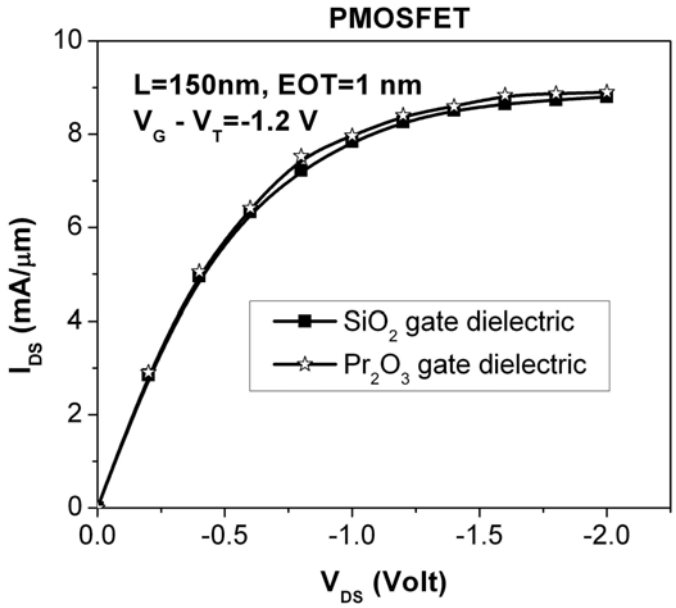

Fig. 6.1: Comparison of drain current characteristics of a PMOSFETs with EOT=1 nm and L=150 nm with different gate dielectrics, SiO_2 and Pr_2O_3.

6.3 Device Characteristics: Alternatively Doped Gate Bulk CMOS Devices

Device characteristics of both NMOSFETs and PMOSFETs with alternatively doped gates and conventionally doped gates were simulated using the device simulator MEDICI. The simulated devices

have an identical threshold voltage of 0.4 V in the case of a NMOSFET and -0.4 V in the case of a PMOSFET. While simulating the device characteristics, unless otherwise explicitly stated, the source and bulk were grounded. The sections that follow include a discussion of the simulated device characteristics in more detail.

6.3.1 Current-Voltage Characteristics

In this section a comparison of device I-V characteristics, drain current characteristics and subthreshold characteristics will be discussed in detail.

6.3.1.1 Drain Current Characteristics

The simulated drain current characteristics of inversely doped gate devices (IDG) and conventionally doped gate devices (CDG) are shown in fig. 6.2 and fig. 6.3 for a NMOSFET and a PMOSFET respectively. The devices have a channel length of 150 nm and equivalent oxide thickness of 2 nm. The gate doping of the devices, primarily differ in gate dopant type and gate doping concentration. The inversely doped gate NMOSFETs have a gate doping of 10^{17} boron atoms per cm^3 and the conventional devices have a gate doping of 10^{19} phosphorus atoms per cm^3 in the case of low doped poly gate devices and 10^{20} phosphorus atoms per cm^3 in the case of highly doped gate devices. Similarly, the inversely doped gate PMOSFETs have a gate doping of 10^{17} phosphorus atoms per cm^3 and the conventional devices have a gate doping of 10^{19} boron atoms per cm^3 in the case of low doped poly gate devices and 10^{20} boron atoms per cm^3 in the case of highly doped gate devices. The device characteristics are simulated at a gate over drive of V_{GS} - V_T=1.2 V in the case of NMOSFETs and V_{GS} - V_T=-1.2 V in the case of PMOSFETs, thus eliminating any small V_T variations.

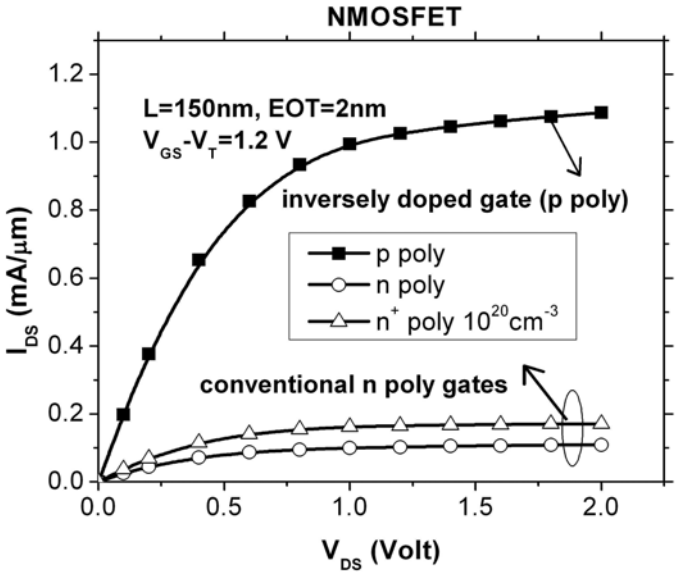

Fig. 6.2: Drain current characteristics of NMOSFETs (L=150 nm, EOT=2 nm) with inversely doped poly gate, low doped n-poly gate and highly doped n-poly gate.

The inversely doped gate devices show a significant performance gain in terms of drain current as shown in fig. 6.2 and fig. 6.3. The NMOSFET with an inversely doped poly gate has an improved gate current when compared to its conventionally doped poly gate counterparts. Similarly

the PMOSFET with a n-poly gate has an improved drain current when compared to its p-poly gate counterparts.

When the drain current characteristics of conventionally doped gate devices were looked at, the devices with a highly doped poly gate have a better drain current characteristics when compared to the devices with lowly doped poly gate. The reason for the improvement in the drain current of high gate doped conventional gate devices can be attributed to the improvement in gate capacitance. The gate capacitance improves in the case of highly doped gates due to the reduction in poly gate depletion, which reduces the poly gate capacitance. This results in gate capacitance improvement and as a result, the drain current of the conventional devices with highly doped poly gate improves.

In the case of inversely doped gate CMOS devices, the improvement in the drain current can be attributed to various reasons. The possible reasons are:

1. gate capacitance improvement
2. gate over drive improvement
3. suppressed RCS
4. mobility enhancement due to reduced V_T adjust implants

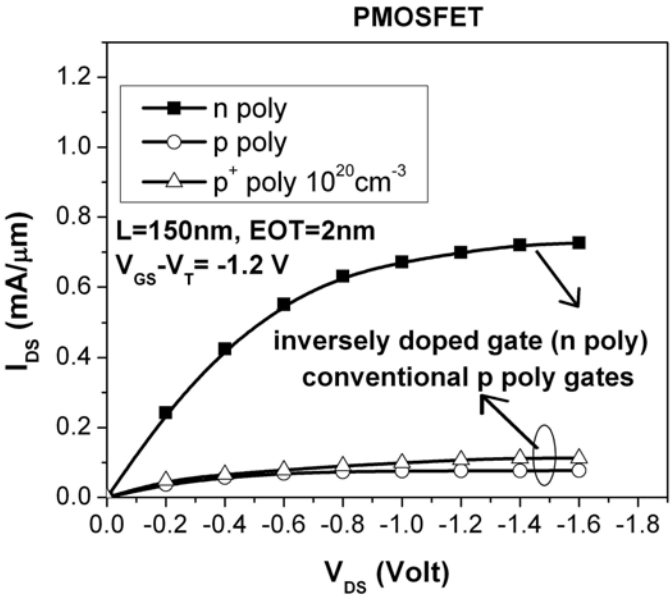

Fig. 6.3: Drain current characteristics of PMOSFETs (L=150 nm, EOT=2 nm) with inversely doped poly gate, low doped n-poly gate and highly doped n-poly gate.

When the gate electrode of the MOSFET is inversely doped, the gate is driven into accumulation when the device is turned on as shown in fig. 5.4. In accumulation, the capacitance can follow the applied gate bias and as a result the gate capacitance is retained at its maximum possible value C_{ox}. The drain current, as well as saturation drain current (I_{DSat}) are directly proportional to the gate capacitance (eqn. (2.38) and eqn. (2.40)), the improved gate capacitance results in increased

drain current and I_{DSat}. In conventionally gate doped devices, when the device is turned on, the gate is driven into depletion. When the gate is biased, part of the applied gate bias drops across the depleted poly [5]. Thus the effective gate bias felt by the channel is reduced. In other words, the gate over drive is reduced. As the gate over drive is directly proportional to the drain current and to square of the gate over drive in case of I_{DSat}, the drain current and I_{DSat} of the CMOS devices with inversely doped poly gate electrodes increases.

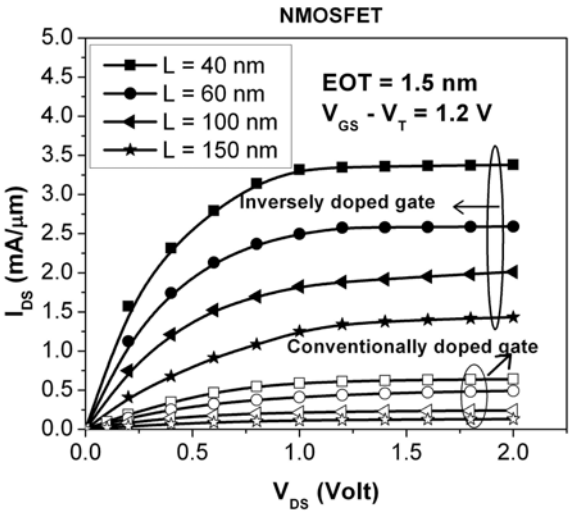

Fig. 6.4: Comparison of drain current characteristics of NMOSFETs with conventionally doped gate devices and with inversely doped gate devices for various channel lengths ranging from 150 nm down to 40 nm.

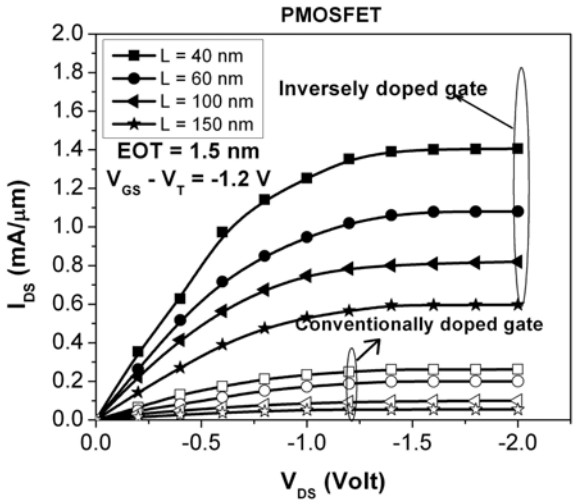

Fig. 6.5: Comparison of drain current characteristics of PMOSFETs with conventionally doped gate devices and with inversely doped gate devices for various channel lengths ranging from 150 nm down to 40 nm.

The improvement in mobility in the case of inversely doped gate devices when compared to the conventionally doped devices can be explained in the following way: when the conventionally gate doped device is turned on, the poly gate gets depleted, due to the gate bias. As a result, a thin depletion layer region is formed at the poly silicon gate-gate oxide interface. The charges in the depleted gate act as parasitic charges centers in the case of conventionally doped gate devices as shown in fig. 2.37. These parasitic charge centers scatter the charge carriers in the channel, thus decreasing the mean free time between collisions $\langle\tau\rangle$. The carrier mobility is a function of the mean free time between collisions and is given as [15]

$$\mu = \frac{q\langle\tau\rangle}{m^*} \tag{6.1}$$

where m^* is the effective mass of the charge carriers. Due to the scattering, the mean free time between the collisions decreases. As a result, from eqn. (6.1), the mobility of the carriers in the channel decreases. From the drain current characteristics eqn. (2.38), it is noticeable that the drain current is directly proportional to the mobility of carriers. Thus, the drain current and I_{DSat} are reduced as a result of the Coulomb scattering in conventionally doped poly gate CMOS devices. In the case of inversely doped poly gate CMOS devices, because the gate is driven into accumulation when the devices are turned on, there are no parasitic gate charges present in the gate electrode. This means that the remote Coulomb scattering of charge carriers in the channel is totally eliminated. As

a result, the drain current in the inversely doped gate devices increases.

The other improvement in mobility is down to the increase in bulk mobility and/or surface mobility as well as the reduction in impurity scattering of the carriers in the channel which is caused by a reduction in channel doping for the inversely doped gate devices. The mobility effect from ionized impurities μ_i can be described as [15]:

$$\mu_i = \frac{64\sqrt{\pi}\varepsilon_0^2\varepsilon_{si}^2(2kT)^{\frac{3}{2}}}{N_A q^3 m^*}\left\{\ln\left[1+\left(\frac{12\pi\varepsilon_0\varepsilon_{si}kT}{q^2 N_A^{\frac{1}{3}}}\right)^2\right]\right\}^{-1} \tag{6.2}$$

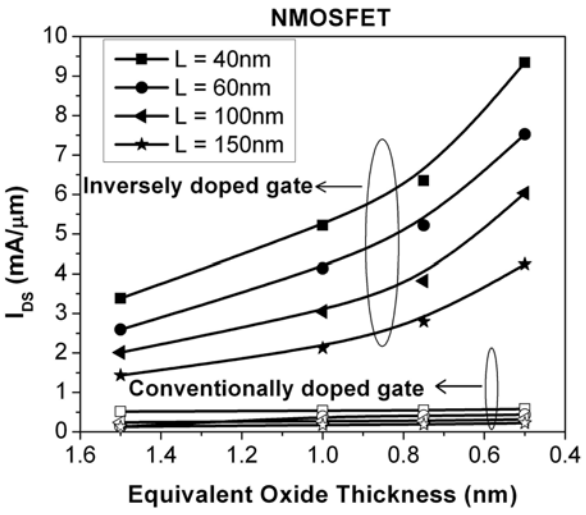

Fig. 6.6: Comparison of drain current characteristics of NMOSFETs with conventionally doped gate devices with NMOSFETs with inversely doped gate devices as a function of equivalent oxide thickness ranging for various channel lengths ranging from 150 nm down to 40 nm.

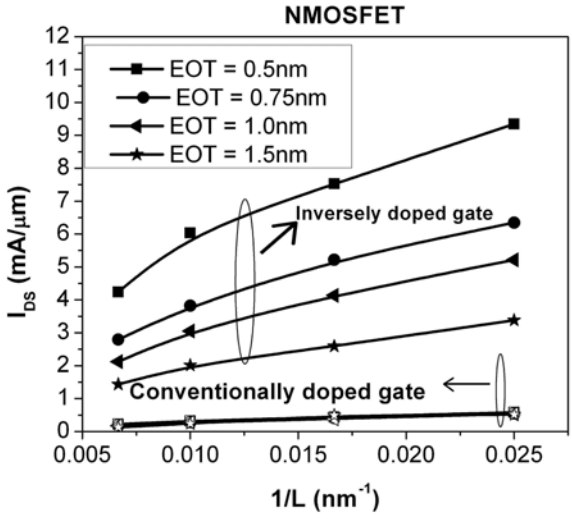

Fig. 6.7: Comparison of drain current characteristics of NMOSFETs with conventionally doped gate devices with NMOSFETs with inversely doped gate devices as a function of channel length for various equivalent oxide thickness ranging from 1.5 nm down to 0.5 nm.

In CMOS devices with conventionally doped gates, the threshold voltage of the devices decreases, due to V_T roll off. To improve the V_T, a V_T adjust implant is made to raise the doping in the channel, as discussed earlier (section 2.7.1.1). The V_T adjust implants are very high so the doping in the channel is the order of about 10^{18} dopant atoms per cm^3. As a result, from eqn. (6.2), it is noticeable that the mobility decreases due to increased channel doping. As the carrier mobility is dependent on the bulk mobility, the high doping in the channel drastically reduces the mobility of the charge carriers in the channel. The mobility reduction is about an order at such a high doping concentrations [15]. The reduced mobility in turn reduces the drain current and saturation drain current in the conventionally doped gate CMOS devices. However, in inversely gate doped CMOS devices, even though the V_T reduces due to V_T roll-off, the threshold voltage in these devices can be adjusted by adjusting the gate work function instead of V_T adjust implants in the channel. As a result, the channel doping is low thus aiding an improvement in the bulk mobility and consequently the surface mobility. The improved mobility aided by the reduced V_T adjust implants thus results in improved drain current and saturation drain current in the case of inversely doped gate CMOS devices when compared to their inversely doped gate counterparts.

When the drain current of conventionally gate doped devices with lowly doped gate and highly doped gate devices are compared, the devices with higher gate doping have better drain current characteristics. The reason being is, that even though the conventionally doped devices with highly doped poly gate need high amounts of V_T adjust implants when compared to their lowly doped counterparts, the resultant mobility doesn't change significantly as in the case of inversely doped gate devices. In addition to this, the gain in mobility in the case of conventionally lowly doped gate devices is over compensated by the loss in gate capacitance. This can be explained in the following fashion. If μ_L and μ_H are the carrier mobilities and C_{GL} and C_{GH} are the gate capacitances for the lowly doped conventional poly gate device and the highly doped conventional poly gate device respectively, then the comparison of saturation drain current at a fixed gate overdrive is given as (form fig. 6.3 it is noticeable that the saturation drain current of a conventionally highly doped poly gate device is more than the conventionally lowly doped poly gate device):

$$\frac{\mu_H C_{GH}}{\mu_L C_{GL}} > 1 \tag{6.3}$$

The improved gate doping improves the poly gate depletion capacitance in highly doped poly device: Thus, $\frac{C_{GH}}{C_{GL}} > 1$. The saturation of mobility at high channel doping results in approximately equal mobility values. Thus the gain in mobility is overcompensated by the loss in gate capacitance caused by the poly gate depletion effect in conventionally lowly doped gate devices.

The studies on the drain current characteristics for inversely doped gate CMOS devices were continued as a function of both channel length and EOT. The drain current characteristics of both NMOSFET and PMOSFET with inversely doped gates and conventionally doped gate devices of

EOT (nm)	I_{DS} (mA/μm)							
	L=150nm		L=100nm		L=60nm		L=40nm	
	IDG	CDG	IDG	CDG	IDG	CDG	IDG	CDG
1.5	1.43	0.131	2.01	0.242	2.59	0.131	3.38	0.514
1.0	2.12	0.177	3.05	0.275	4.14	0.390	5.22	0.540
0.75	2.79	0.189	3.82	0.281	5.22	0.409	6.35	0.546
0.50	4.24	0.223	6.04	0.318	7.52	0.437	9.34	0.582

Table 6.2: Variation of saturation drain current I_{DSat} of NMOSFETs with inversely doped gates and conventionally doped gates as a function of channel length and EOT at a gate bias of 1.2 V and drain bias of 2.0 V.

different channel length ranging from 150 nm down to 40 nm with an equivalent oxide thickness of 1.5 nm are shown in fig. 6.4 and fig. 6.5 respectively. Fig. 6.6 and fig. 6.7 show the drain current comparisons of NMOSFETs with inversely doped gate devices and conventionally doped gate devices with various channel lengths and EOT at a drain bias of V_{DS}=2.0 V and a gate bias of V_{GS}=1.2 V. Fig. 6.8 and fig. 6.9 show the drain current comparisons of PMOSFETs with inversely doped gate devices and conventionally doped gate devices with various channel lengths and EOT at a drain bias of V_{DS}=-2.0 V and a gate bias of V_{GS}=-1.2 V. Table 6.2 and 6.3 give an overview of the drain current (at $|V_{DS}|$=2.0 V, $|V_{GS}|$=1.2 V) variations of both NMOSFETs and PMOSFETs with inversely doped gates and conventionally doped gates when channel length and equivalent oxide thickness are changed. It has been found that the inversely doped gate devices have a significant performance improvement in terms of drain current when compared to their conventionally doped

counterparts in the case of both NMOSFETs and PMOSFETs.

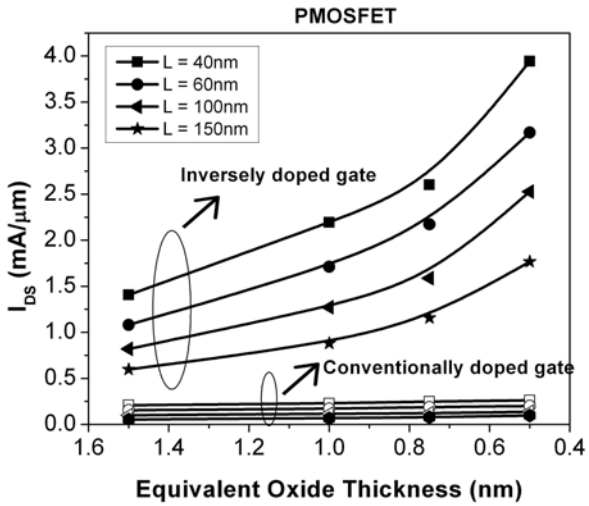

Fig. 6.8: Comparison of drain current characteristics of PMOSFETs with conventionally doped gate devices with PMOSFETs with inversely doped gate devices as a function of equivalent oxide thickness ranging for various channel lengths ranging from 150 nm down to 40 nm.

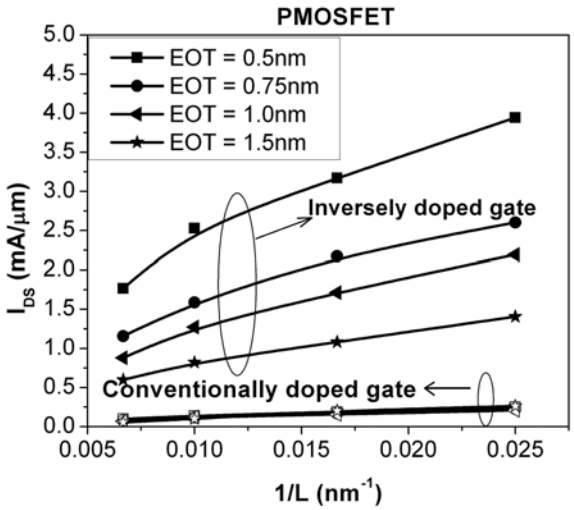

Fig. 6.9: Comparison of drain current characteristics of PMOSFETs with conventionally doped gate devices with PMOSFETs with inversely doped gate devices as a function of channel length for various equivalent oxide thickness ranging from 1.5 nm down to 0.5 nm.

EOT (nm)	I_{DS} (mA/μm)							
	L=150nm		L=100nm		L=60nm		L=40nm	
	IDG	CDG	IDG	CDG	IDG	CDG	IDG	CDG
1.5	0.597	0.0544	0.820	0.100	1.08	0.155	1.41	0.209
1.0	0.880	0.0672	1.27	0.117	1.71	0.170	2.19	0.228
0.75	1.16	0.0785	1.59	0.121	2.17	0.188	2.60	0.250
0.50	1.77	0.0971	2.53	0.138	3.12	0.200	3.94	0.262

Table 6.3: Variation of saturation drain current I_{DSat} of PMOSFETs with inversely doped gates and conventionally doped gates as a function of channel length and EOT at a gate bias of -1.2 V and drain bias of -2.0 V.

Furthermore, to study the effect of the inversely doped gate architectures on the drain currents, the saturation drain current ratios were investigated. The ratio of the saturation drain current of NMOSFETs with inversely doped gates ($I_{DSat}IDG$) to the saturation drain current of NMOSFETs with conventionally doped gates ($I_{DSat}CDG$), i.e, $\frac{I_{DSat}IDG}{I_{DSat}CDG}NMOSFET$, was compared with the ratio $\frac{I_{DSat}IDG}{I_{DSat}CDG}PMOSFET$. The comparisons are tabulated in table 6.4. Generally, this ratio is found to be more in case of the NMOSFETs than in the case of PMOSFETs. This observation can be explained in the following fashion. In silicon, the mass of electrons is less when compared to the mass of holes [80]. So higher electrical fields are required to scatter the holes in the channel when compared to the electric fields required to scatter the electrons in the channel. As a result, the device degradation caused by RCS is less in the case of PMOSFETs while the degradation due to RCS is more in the

case of NMOSFETs. This results in higher saturation drain currents in the case of conventionally doped gate PMOSFETs. The individual factor which assist in the improvement of drain current

L	I_{Dsat}IDG/I_{Dsat}CDG			
	EOT =0.75nm		EOT =0.50nm	
	NMOSFET	PMOSFET	NMOSFET	PMOSFET
150	14.8	14.8	19	18.2
100	13.6	13.1	18.9	18.3
60	12.8	11.5	17.2	15.6
40	11.6	10.4	16.4	15

Table 6.4: Comparison of the ratio I_{DSat}IDG/I_{DSat}CDG of NMOSFETs with the ratio I_{DSat}IDG/ I_{DSat}CDG of PMOSFETs as a function of channel length and EOT at a gate bias of |1.2V| and drain bias of |2.0V|.

characteristics are caused approximately 4 times by the eliminated gate depletion and 2 times caused by the increased carrier mobility due to suppressed RCS (section 6.6). The reduced channel doping in inversely doped gate devices accounts for the further improvement in mobility. Thus resulting in the estimated performance improvement.

6.3.1.2 Subthreshold Characteristics

The simulated subthreshold characteristics of inversely doped gate devices and conventionally doped gate devices are shown in fig. 6.10 and fig. 6.11 for a NMOSFET and PMOSFET respectively. The devices have a channel length of 150 nm and equivalent oxide thickness of 2 nm. While simulating the subthreshold characteristics, the drain to source voltage V_{DS} is kept at 0.4 V in the case of NMOSFETs and -0.4 V in the case of PMOSFETs. When the subthreshold characteristics are compared, the devices with an inversely doped gate have higher off currents. This is due to having less control

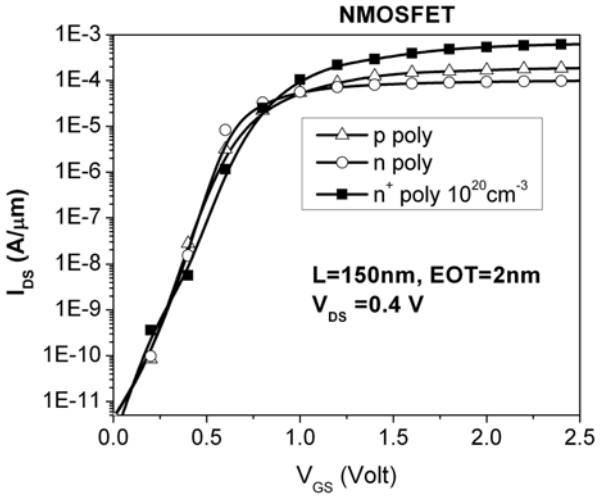

Fig. 6.10: Comparison of subthreshold characteristics of NMOSFETs with inversely doped gate and conventionally highly doped poly gates and conventionally lowly doped poly gates.

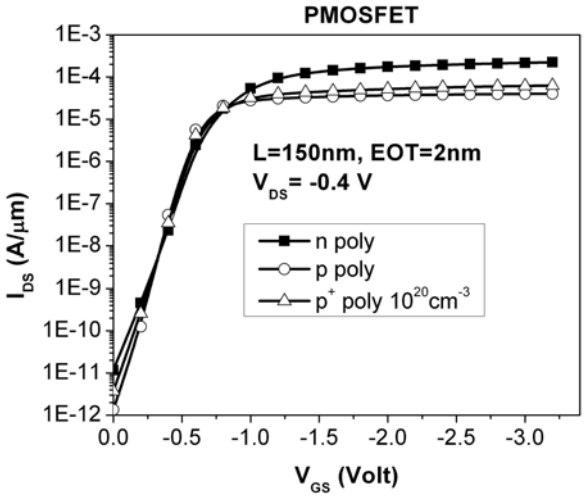

Fig. 6.11: Comparison of subthreshold characteristics of PMOSFETs with inversely doped gate and conventionally highly doped poly gates and conventionally lowly doped poly gates.

over the gate when the device is turned off. When the device is turned off, the gate bias causes the gate to deplete and thus resulting in less control over the channel region. However, these devices have a good subthreshold slope of around 85 mV/decade. The leakage current has been improved with an increasing gate doping concentration for inversely doped gate devices. This suggests that the devices with high gate doping concentration have a better control over the gate. The gate doping improvement of inversely doped gate devices is discussed in section 6.3.3.

6.3.2 A.C. Characteristics

In this section the a.c. characteristics of the CMOS devices, namely transconductance and cutoff frequency will be discussed.

6.3.2.1 Transconductance

The subthreshold characteristics were used to extract the transconductance of the devices. In this section, the transconductance characteristics of CMOS devices down to an EOT of 0.5 nm and channel length of 40 nm will be looked at. The transconductance characteristics of a NMOSFET with inversely doped gate, a conventionally highly doped poly gate and a conventionally lowly doped poly gate are shown in fig. 6.12. While fig. 6.13 shows the transconductance characteristics of a PMOSFET with inversely doped gate and conventionally highly doped poly gate and conventionally lowly doped poly gate. The channel length and EOT of these devices are 150 nm and 2 nm respectively, while the device width is assumed to be 1 μm. The drain is biased at 0.4 V in the case of NMOSFET and -0.4 V in case of PMOSFET, while the gate bias is varied.

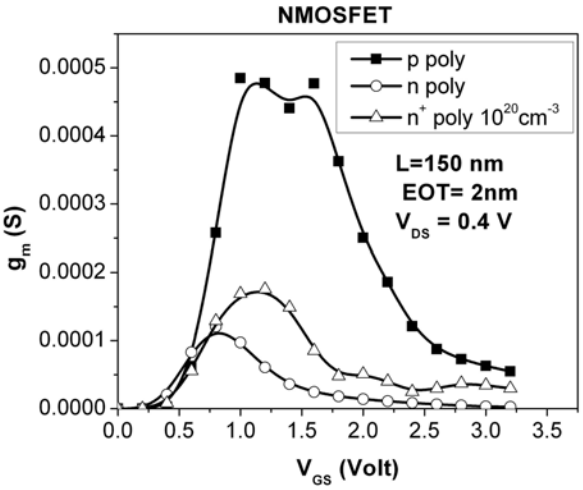

Fig. 6.12: Comparison of transconductance (g_m) of NMOSFETs with inversely doped gate, conventionally highly doped poly gate and conventionally lowly doped poly gate.

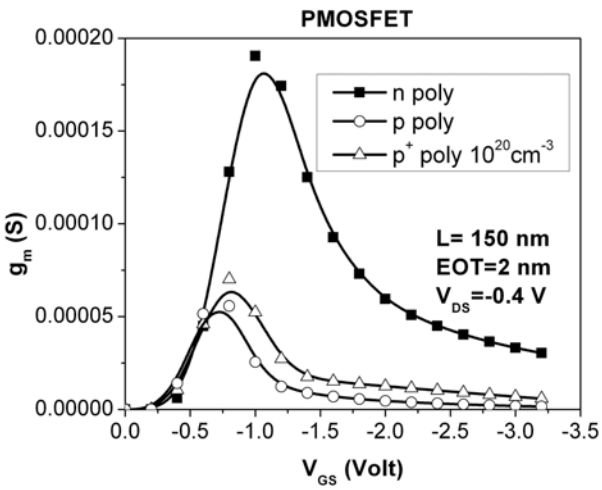

Fig. 6.13: Comparison of transconductance (g_m) of PMOSFETs with inversely doped gate, conventionally highly doped poly gate and conventionally lowly doped poly gate.

The transconductance of both NMOSFETs and PMOSFETs with inversely doped gates is improved significantly when compared to their conventionally doped counterparts. The improvement in the transconductance in the case of inversely doped gates can be attributed to the improved mobility.

The variation of transconductance of NMOSFETs as a function of channel length for different equivalent oxide thickness values were compared in fig. 6.14 for inversely doped gates (IDG) and conventionally doped gates (CDG). The variation of transconductance of NMOSFETs as a function of

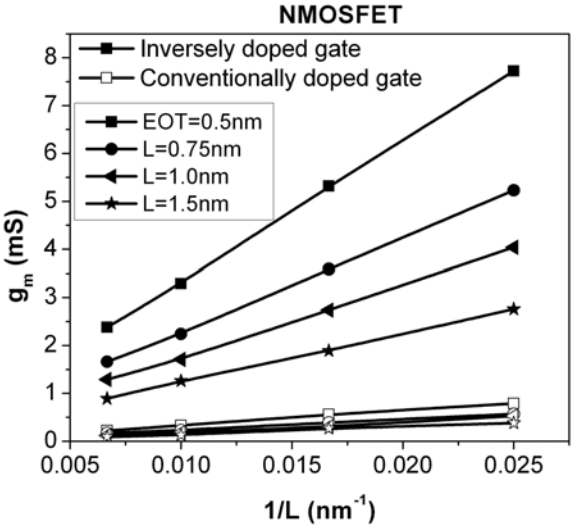

Fig. 6.14: Variation of transconductance (g_m) of NMOSFETs with inversely doped gates and conventionally highly doped poly gates as a function of channel length.

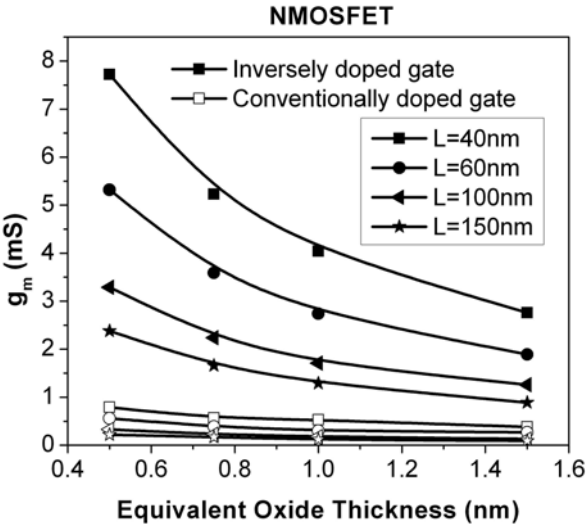

Fig. 6.15: Variation of transconductance (g_m) of NMOSFETs with inversely doped gates and conventionally highly doped poly gates as a function of EOT.

equivalent oxide thickness for different channel length values were compared in fig. 6.15 for inversely doped gates (IDG) and conventionally doped gates (CDG) and are tabulated in table 6.5. The variation of transconductance of NMOSFETs as a function of channel length for different equivalent oxide thickness values were compared in fig. 6.16 for inversely doped gates (IDG) and conventionally doped gates (CDG). The variation of transconductance of NMOSFETs as a function of equivalent oxide thickness for different channel length values were compared in fig. 6.17 for inversely doped

EOT (nm)	Transconductance (g_m (mS))							
	L=150 nm		L=100 nm		L=60 nm		L=40 nm	
	IDG	CDG	IDG	CDG	IDG	CDG	IDG	CDG
1.5	0.89	0.092	1.26	0.13	1.89	0.27	2.76	0.38
1.0	1.29	0.12	1.71	0.18	2.74	0.30	4.04	0.53
0.75	1.66	0.17	2.24	0.23	3.59	0.39	5.23	0.57
0.50	2.38	0.22	3.29	0.33	5.32	0.56	7.72	0.79

Table 6.5: Transconductance (g_m) values of NMOSFETs with inversely doped gates and conventionally doped gates as a function of channel length and EOT.

gates (IDG) and conventionally doped gates (CDG) and are tabulated in table 6.6. It has been discovered that the CMOS device with inversely doped gates have an improved transconductance values when compared to their conventionally doped gate counterparts. The improved g_m results in a better cutoff frequency characteristics.

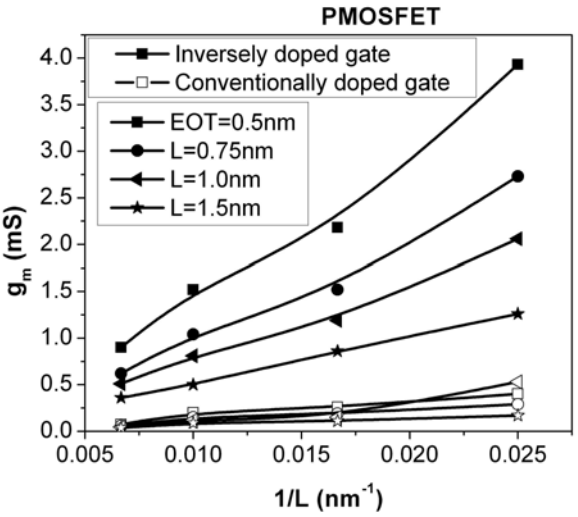

Fig. 6.16: Variation of transconductance (g_m) of PMOSFETs with inversely doped gates and conventionally highly doped poly gates as a function of channel length.

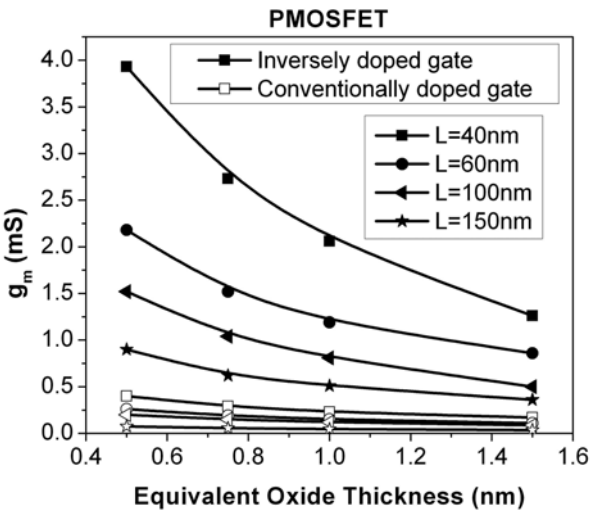

Fig. 6.17: Variation of transconductance (g_m) of PMOSFETs with inversely doped gates and conventionally highly doped poly gates as a function of EOT.

EOT (nm)	Transconductance (g_m (mS))							
	L=150 nm		L=100 nm		L=60 nm		L=40 nm	
	IDG	CDG	IDG	CDG	IDG	CDG	IDG	CDG
1.5	0.36	.036	0.50	0.089	0.86	0.11	1.26	0.17
1.0	0.51	0.045	0.81	0.12	1.19	0.15	2.06	0.23
0.75	0.62	0.057	1.04	0.15	1.52	0.19	2.73	0.29
0.50	0.90	0.075	1.52	0.195	2.18	0.26	3.93	0.40

Table 6.6: Transconductance (g_m) values of PMOSFETs with inversely doped gates and conventionally doped gates as a function of channel length and EOT.

6.3.2.2 Cutoff Frequency

Table 6.7 lists the cutoff frequency of NMOSFETs with inversely doped gates and conventionally doped gates while table 6.8 lists the the cutoff frequency of PMOSFETs with inversely doped gates

EOT (nm)	f_T (GHz)							
	L=150 nm		L=100 nm		L=60 nm		L=40 nm	
	IDG	CDG	IDG	CDG	IDG	CDG	IDG	CDG
1.5	36.6	4.40	75.8	9.32	204	32.3	444	68.2
1.0	38.2	5.47	77.4	12.3	206	34.2	452	80.6
0.75	39.6	6.82	78.8	13.8	210	39.1	465	85.8
0.5	41.0	7.84	87.11	17.6	218	49.9	477	106

Table 6.7: Cutoff frequency (f_T) of NMOSFETs with inversely doped gates and conventionally doped gates as a function of channel length and EOT.

and conventionally doped gates. For evaluating the cutoff frequency, the maximum transconductance

values are used. The increase in cutoff frequency is very significant and with channel lengths of 40nm, the cutoff frequency of devices almost reaches THz (10^{12} Hz). As a result of high cutoff frequencies, these devices are more suitable for RF applications and high performance microprocessor applications.

EOT (nm)	f_T (GHz)							
	L=150 nm		L=100 nm		L=60 nm		L=40 nm	
	IDG	CDG	IDG	CDG	IDG	CDG	IDG	CDG
1.5	13.8	1.72	34.5	6.38	83.7	13.2	218	30.5
1.0	14.3	2.05	35.0	8.21	87.5	17.1	226	39.3
0.75	15.7	2.29	35.9	9.03	91.4	19.1	235	43.6
0.5	16.6	2.67	37.3	10.4	99.0	21.1	237	53.5

Table 6.8: Cutoff frequency (f_T) of PMOSFETs with inversely doped gates and conventionally doped gates as a function of channel length and EOT.

6.3.3 Gate Doping Dependency of Inversely Doped Gate Devices on Channel Length

In conventionally doped devices, low gate doping levels 10^{17} cm^{-3} result in high gate resistivity of the gate electrode. The high resistivity of the gate results in a voltage drop across the gate electrode. This is a deviation from the requirement of having a low resistive gate electrode. In order to decrease the gate resistivity, the gate doping should be increased. The increased gate doping thus effects the work function of the gate and as a result, the threshold voltage changes. However, the gate electrode conductivity can be increased by gate poly silicidation [81], [82]. The silicidation of the poly gate improves the gate conductivity without effecting the threshold voltage of the device.

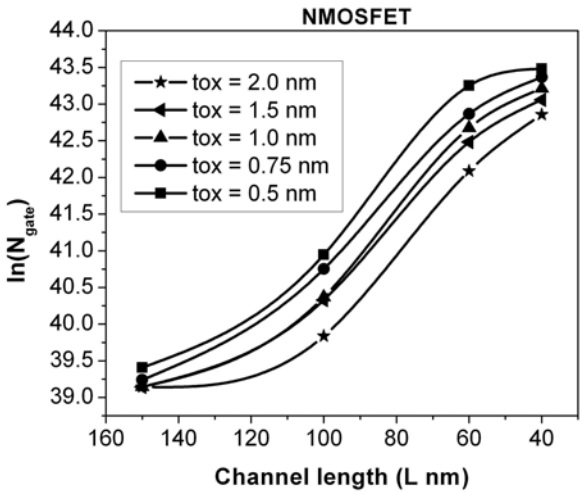

Fig. 6.18: Variation of gate doping in inversely doped gate NMOSFETs as a function of channel length.

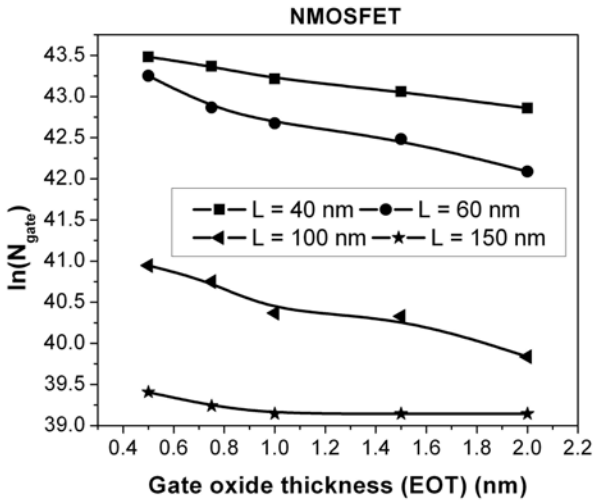

Fig. 6.19: Variation of gate doping in inversely doped gate NMOSFETs as a function of equivalent oxide thickness.

The V_T roll-off in short channel CMOS devices needs threshold voltage adjustments. Instead of adjusting the V_T by channel implants, the gate work function can be increased. The increment

in gate work function results into an increment in gate doping concentration. As a result, the gate resistivity decreases. The gate doping concentration improvement of both NMOSFETs and PMOSFETs was studied in detail. The variation of gate doping as a function of channel length and EOT of NMOSFETs are shown in fig. 6.18 and fig. 6.19 respectively and are tabulated in table 6.9.

EOT(nm)	Gate doping (10^{18}cm^{-3})			
	L=150 nm	L=100 nm	L=60 nm	L=40 nm
1.5	0.10	0.313	2.58	4.90
1.0	0.10	0.32	2.72	5.56
0.75	0.10	0.42	3.17	6.47
0.50	0.11	0.50	4.14	6.82

Table 6.9: Variation of gate doping in inversely doped gate NMOSFETs as a function of channel length equivalent oxide thickness.

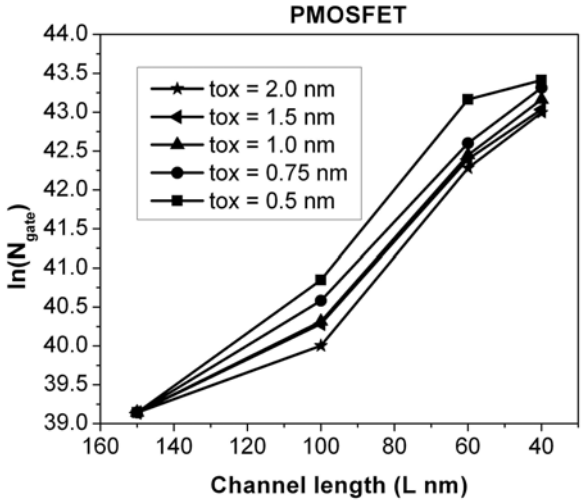

Fig. 6.20: Variation of gate doping in inversely doped gate PMOSFETs as a function of channel length.

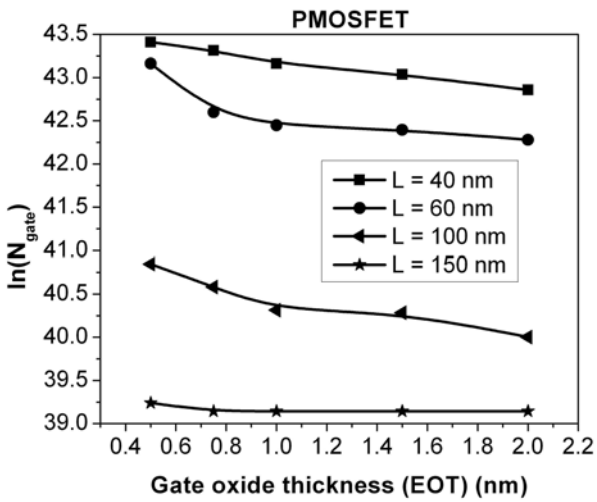

Fig. 6.21: Variation of gate doping in inversely doped gate PMOSFETs as a function of equivalent oxide thickness.

EOT(nm)	Gate doping (10^{18}cm^{-3})			
	L=150 nm	L=100 nm	L=60 nm	L=40 nm
1.5	0.10	0.313	2.58	4.90
1.0	0.10	0.32	2.72	5.56
0.75	0.10	0.42	3.17	6.47
0.50	0.11	0.50	4.14	6.82

Table 6.10: Variation of gate doping in inversely doped gate PMOSFETs as a function of channel length equivalent oxide thickness.

For a PMOSFET the gate doping variations are shown in fig. 6.20 and fig. 6.21 respectively as a function of channel length and EOT and are tabulated in table 6.10. The improved gate doping

results not only in reduced gate electrode resistance but also in a better control over the gate when the device is turned off. This results in improved device subthreshold characteristics and off state characteristics which is a discrete advantage in low standby power devices and memory devices.

6.4 Device Fabrication

The device simulations suggest that the device performance can be improved with inversely doped gate devices. In order to prove the concept of inversely doped gate devices right, suitable hardware was fabricated. Inversely doped gate buried channel PMOSFETs with a channel length of 1.2μm and EOT of 9nm were fabricated with a gate doping concentrations of 10^{18} phosphorus atoms cm^{-3} and 10^{20} phosphorus atoms cm^{-3}.

6.4.1 Device Characteristics: Measurements

The fabricated PMOSFETs were then used to obtain the device characteristics namely, drain current characteristics and subthreshold characteristics. The drain current of the devices, shown in fig. 6.22 was obtained at two different gate voltages (V_G) -1 V and -2 V. From the drain current characteristics, it is noticeable that the saturation drain current of the inversely doped devices with low gate doping is high when compared to the saturation drain current of the devices with high gate doping. The reason for improved drain current in the case of low doped gate devices is that, they need low V_T adjust implants, which help to improve the mobility.

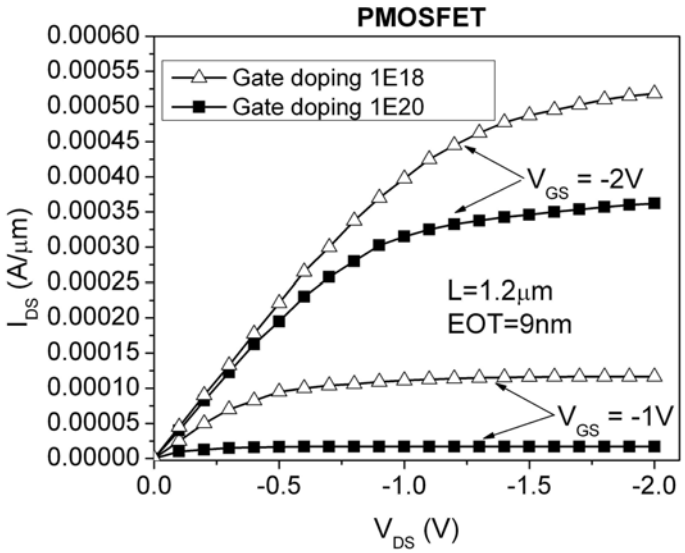

Fig. 6.22: Measured drain current characteristics of a inversely doped gate PMOSFETs.

The subthreshold characteristics of inversely doped devices is shown in fig 6.23. The subthreshold slope in the case of highly doped gate devices is 80 mV/dec, while that of lowly doped gate devices is 85 mV/dec. The device with high gate doping concentration has less off state leakage when compared to the devices with low gate doping concentration which can be inferred from the lower part of the

subthreshold characteristics curve. The reason for better off-state characteristics in the case of a highly doped gate can be attributed to the depleted gate of the device, when the device is turned off. The gate depletion degrades the control over the channel region in off state in both of the highly doped and lowly doped gate devices. However, due to reduced poly gate depletion in the case of highly doped inversely doped gate devices, these devices have a better control over the channel region when compared to their lowly doped counterparts, resulting in less off-state leakage.

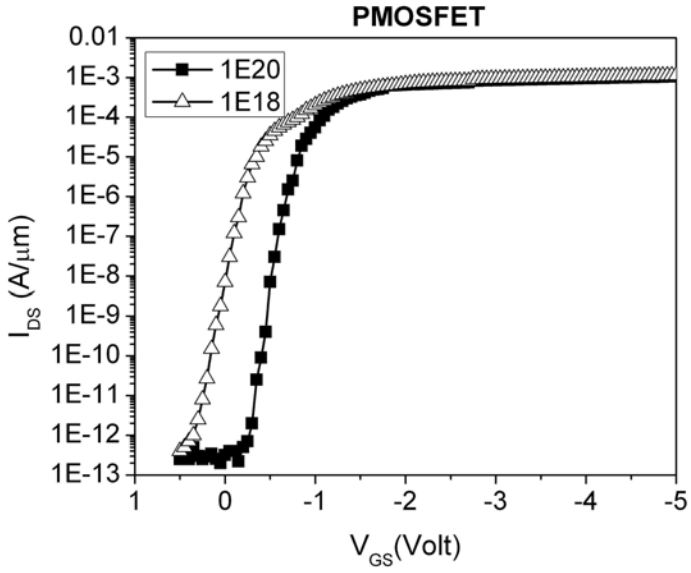

Fig. 6.23: Measured subthreshold characteristics of a inversely doped gate PMOSFETs.

Thus considering the drain current characteristics, it is obvious that low gate doping concentration is required for high drive currents. While, from the subthreshold characteristics point of view, a high doping concentration is needed for better off-state characteristics. Thus an optimization is needed on gate doping concentration to obtain good drain current characteristics while keeping the off state current as low as possible. The dependency of gate doping on channel lengths, i.e, as discussed in section 6.3.3, the increment of gate doping levels with decreasing channel lengths aids to the cause, resulting in a better subthreshold performance of the devices.

In inversely doped gate devices, the threshold voltage of the device can be adjusted either by gate doping optimization or by adjusting the channel doping. The gate optimization should be performed according to how the device is used. For example, in the case of memories, less device leakage currents are more important, as high leakage currents reduce the retention times and thus need more/faster memory refresh cycles. From the measured subthreshold characteristics, the inversely doped gate devices with low gate doping have less gate leakage, while the devices with low gate doping have high leakages. Thus in the case of memories high gate doping is required. In the case of logic gates, a bad subthreshold slope effects the switching characteristics of the logic circuit, while high drive current is required. As a result, optimization of both gate doping for better sub threshold slope and optimization of channel doping for high drive currents is required. In case of RF circuits, a better device optimization is required as high leakage currents increase the noise to signal ratio, while low drain currents decrease the transconductance thus decreasing the device cutoff frequency. However,

a high subthreshold slope results in high leakage currents which degrades the device characteristics. So an optimization in device architecture is needed which is highly dependent on how the device is used.

While simulating the inversely doped gate CMOS devices, the substrate doping is held at 10^{16} dopant atoms cm^{-3}. Low substrate doping can result in source-drain punch through and accelerated short channel effects. The source drain punch through and the accelerated short channel effects can be minimized by using a retrograde channel profile [83], [84], [85]. Another option to suppress source/drain punch through and to suppress short channel effects is to use SOI structures. The device characteristics via simulations confirm the performance improvement of SOI CMOS devices with inversely doped gate architectures as, discussed in section 6.5.

6.5 Device Characteristics: FDSOI CMOS Devices

In this section the device characteristics of fully depleted silicon on insulator CMOS devices will be discussed. Both FD-SOI NMOSFETs and FD-SOI PMOSFETs have a channel length of 150 nm and equivalent oxide thickness of 2.0 nm. The devices have a threshold voltage of 0.4 V in the case of FD-SOI-NMOSFETs and -0.4 V in the case of FD-SOI-PMOSFETs.

The drain current characteristics of FD-SOI-NMOSFETs with inversely doped gate devices and

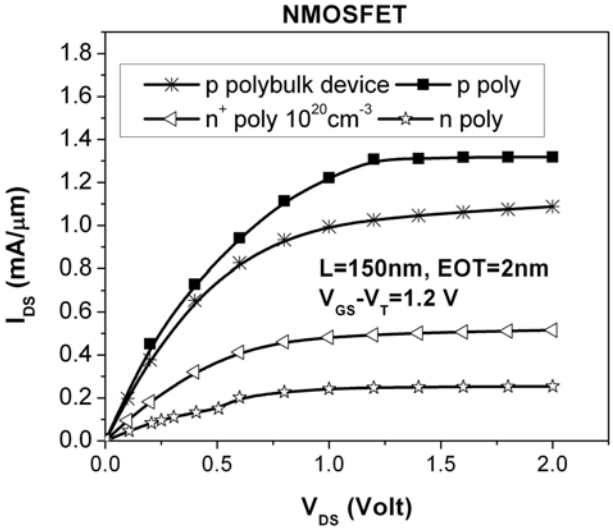

Fig. 6.24: Drain current characteristics of FD-SOI-NMOSFET with an inversely doped gate and conventionally doped gates.

conventionally doped gate devices are shown in fig. 6.24. The FD-SOI NMOSFETs with inversely doped gate devices show improved performance when compared to their conventionally doped counterparts. When the drain current characteristics of bulk NMOSFETs with inversely doped gate devices are compared with drain current characteristics of FD-SOI NMOSFETs with inversely doped gate devices, FDSOI devices show a better performance. The subthreshold characteristics of FD-SOI-NMOSFETs with inversely doped gates and conventionally doped gates are shown in fig. 6.25. The transconductance characteristics of NMOSFETs with inversely doped gates and conventionally

doped gates are shown in fig. 6.26. The transconductance of FD-SOI-NMOSFET with inversely doped gates is $0.67 \times 10^{-3}\,\Omega^{-1}$ when compared to the transconductance value $0.48 \times 10^{-3}\,\Omega^{-1}$ of bulk NMOSFET with an inversely doped gate. In the case of FD-SOI-PMOSFET with inversely doped gates, the transconductance is $0.24 \times 10^{-3}\,\Omega^{-1}$ when compared to the transconductance value $0.18 \times 10^{-3}\,\Omega^{-1}$ of bulk PMOSFET with inversely doped gates. The cutoff frequency of the FD-SOI-NMOSFET with an inversely doped gate is 0.41 THz and 0.30 THz in case of bulk NMOSFET. While the cutoff frequency of the FD-SOI-PMOSFET with inversely doped gate is 0.15 THz and 0.12 THz in the case of bulk PMOSFET. The recently reported cutoff frequency FDSOI NMOSFET with a channel length of 20 nm has a cutoff frequency of 1.4 THz at a drain bias of 0.75 V [86].

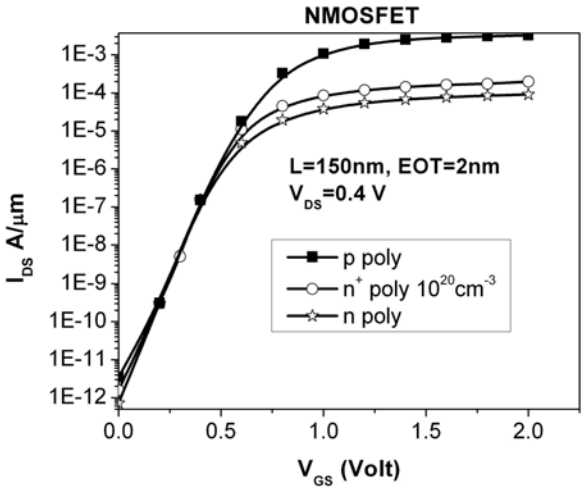

Fig. 6.25: Subthreshold characteristics of FD-SOI-NMOSFET with an inversely doped gate and conventionally doped gates.

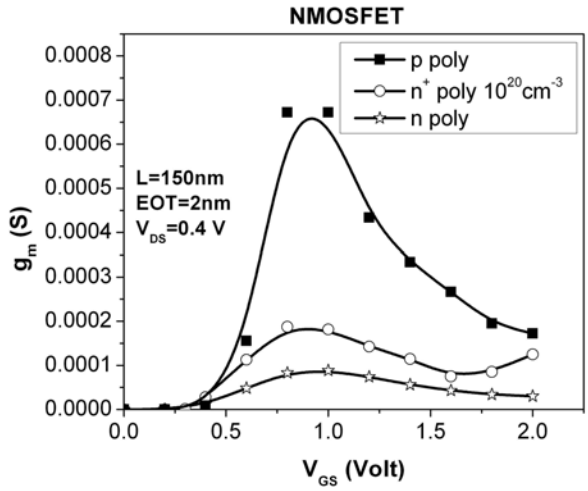

Fig. 6.26: Transconductance characteristics of FD-SOI-NMOSFET with an inversely doped gate and conventionally doped gates.

The improvement in the device performance of FDSOI CMOS devices over bulk CMOS devices can be partly attributed to the improvement in body factor of the devices. When the device equations of bulk devices for drain current eqn. (2.40), for subthreshold slope eqn. (2.55), for transconductance eqn. (2.60) and for cutoff frequency eqn. (2.63) are compared with the device characteristics of SOI devices eqn. (3.16), eqn. (3.18), eqn. (3.19) and eqn. (3.20) for drain current, subthreshold slope, transconductance and cutoff frequency respectively, low body effect coefficient results in better device performance in the case of FDSOI devices.

The simulation results of FD-SOI CMOS devices with inversely doped gate architectures indicate that the device performance which was obtained in the case of inversely doped gate bulk CMOS devices can be achieved even in the case of FD-SOI devices.

6.6 Comparison of Metal Gate Devices and Conventionally Doped Gate Devices

The mobility degradation caused by remote Coulomb scattering due to parasitic charges in the poly gate can be studied by using a metal gate electrode. The metal gate electrode is chosen as such so that the work function of the metal gate is equal to the work function of the poly gate, resulting in identical devices. The only difference is that, the MOSFETs with a metal gate is depletion free while

the MOSFETs with poly silicon gates are depleted. The effective carrier mobility of the metal gate devices(μ_M) were compared with the effective carrier mobility of the poly gate devices(μ_P) at a gate electric field of 8 MV/cm at a fixed drain to source bias of 0.4 V. This comparison resulted in the reduction of effective mobility in carrier mobility due to RCS. The effective mobility enhancement $\frac{\mu_M}{\mu_P}$, for both bulk NMOSFETs and PMOSFETs with a channel length of 100 nm with varying EOT is tabulated in table 6.11 . It is noticeable that the mobility enhancement is greater in the case of

EOT (nm)	NMOSFET	PMOSFET
1.0	1.32	1.21
0.75	1.59	1.48
0.50	1.93	1.69

Table 6.11: Comparison of effective mobility of bulk NMOSFETs and PMOSFETs with metal gate electrode and conventionally doped gate electrode.

NMOSFETs when compared to PMOSFETs, as predicted earlier. Also the mobility enhancement increases with decreasing EOT, which indicates that the remote Coulomb effects becomes more significant in ultra thin oxide systems.

6.7 Processing Requirements for Inversely Doped Gate Devices

The advantage of alternately doped gate electrode devices over the metal gate electrode devices is that these technologies do not need any extra mask levels and replacement gate technologies, which are required in metal gate electrodes [87], [88]. In modern CMOS devices, the high energy gate doping implantation differs low energy source/drain implantations, due to the source/drain junction depth limitations. In conventionally doped CMOS devices, the poly gate can take the source/drain implant dose as the source and drain have the same dopant type when compared to the gate. In the case of inversely doped gate devices, the gate should should be masked while implanting the source and drain regions. The gate masking can be achieved by etching the oxide after the source and drain implants rather than before the implants as the dopant type in source/drain are different for the poly gate dopant type. One more advantage in the case of inversely doped gate devices is that, high temperature processing steps are allowed even after the gate electrode deposition, which are not allowed in case of metal gate electrodes.

6.8 Conclusions

Conventionally doped poly gate CMOS devices suffer with severe poly gate depletion effects. The poly gate depletion effect reduces the gate capacitance and as a result the drain device performance degrades significantly. To reduce poly gate depletion effects, the gate poly can be highly doped. However, due to the gate parasitic charges, the highly doped poly gate degrades the device performance by reducing its mobility, known as remote Coulomb scattering. Thus in conventionally doped gate devices one of the effects, poly gate depletion or RCS is unavoidable. Even though the gate is very highly doped, the poly gate depletion effect is unavoidable when the EOT of the devices is scaled down below 1 nm. In order to improve the performance, metal gates can be used instead of conventionally doped poly gates but integration of metal gates is very difficult. Instead of metal gates, in this work, we used inversely doped gate architectures instead of conventionally doped gate

architectures, i.e., the gate doping type in the devices is changed. As a result, the poly gate depletion was eliminated and RCS is also suppressed. The concept of inversely doped gate devices was demonstrated via extensive simulation studies and the concept was verified with suitable hardware. Using inversely doped gates resulted in a significant performance improvement in terms of drain current, subthreshold slope, transconductance and cutoff frequency in bulk CMOS devices and FDSOI CMOS devices. The performance improvement is attributed to the improvement in gate capacitance, suppressed remote Coulomb scattering effects and increase in effective mobility.

7
Summary and Conclusions

In this work, different gate electrode structures were studied using process and device simulations. It is found via simulations and verified by measurements that inversely doped gate devices gain in performance when compared to their conventionally doped counterparts.

One of the primary aims of device scaling is to improve the device performance. While scaling the channel length of the device into deca nanometer regime, gate insulator also needs to be scaled down. The thinning of gate insulator results in higher gate leakage currents. This issue is being resolved by introducing different gate insulators whose dielectric constant is higher than that of SiO_2. In conventional poly gate CMOS technologies, scaling down the gate insulator thickness results in reduction of gate capacitance due to poly gate depletion when the device is turned on and the reduced gate capacitance results in a degraded device performance. Poly gate depletion results in parasitic gate charge carriers at the gate poly-gate oxide interface. These parasitic gate charges result in remote Coulomb scattering of charge carriers in the channel, which further degrades the device performance.

A novel gate poly doping scheme is suggested in this work, where the gate poly is inversely doped, meaning the gate is doped p-type for a NMOSFET instead of a n-type doping. When an inversely gate doped architecture is used, the poly gate is driven into accumulation when the device is turned on thus completely eliminating the poly gate depletion and remote Coulomb scattering. The concept of inversely dope gate structure is verified by simulations studies. CMOS devices of various channel lengths and equivalent oxide thickness were process simulated. The process simulated structures were then used to simulate the device characteristics. A comparison between the conventionally doped poly gate devices and inversely doped poly gate structures indeed indicates a performance gain. The simulations are then verified using processed hardware.

The concept of inversely doped poly gate structures is then implemented on FDSOI CMOS devices. The simulation studies show similar results when compared to the bulk CMOS devices.

Based on the results presented in this work, with further optimization, the inversely doped gate architectures can be implemented in both low performance and high performance technologies.

List of publications

Conference papers

1. **R. Komaragiri** and U. Schwalke; Depletion-Free Poly Gate Electrode Architecture for Sub 100 Nanometer CMOS Devices with High-K Gate Dielectrics, pp. 705-709, Semiconductor Advances for Future Electronics (SAFE 2005), Veldhoven, The Netherlands, November 2005.

2. Y. Stefanov, **R. Komaragiri** and U. Schwalke; Technological Advances for Memory Applications: Crystalline High-K Gate Dielectrics and Alternatively Doped Gates, p. 167, International Conference on Memory Technology and Design, France, May 2005.

3. **R. Komaragiri**, F.Zaunert, U.Schwalke; Gate Engineering for High-k Dielectric and Ultra-Thin Gate Oxide CMOS Technologies, pp. 108-112, Semiconductor Advances for Future Electronics (SAFE 2004), Veldhoven, The Netherlands, 24th-25th November 2004.

4. Y. Stefanov, **R. Komaragiri**, U.Schwalke; Device Level and Nanoscale Electrical Characterization of Crystalline Praseodymium Oxide High-k Gate Dielectric MOSFETs, SEMATECH International Workshop on Electrical Characterization and Reliability for High-K Devices, Austin, Texas, USA.

5. Y.Stefanov, **R. Komaragiri**, T.Ruland, U.Schwalke Electrical AFM Measurements for STI CMP Erosion Evaluation, Seeing at the Nanoscale II International Conference Abstracts p. 97, Grenoble, France 13th 15th October, 2004.

6. H.D.B. Gottlob, M.C. Lemme, T. Mollenhauer, T. Wahlbrink, J.K. Efavi, H. Kurz, Y. Stefanov, K. Haberle, **R. Komaragiri**, T. Ruland,F. Zaunert, U. Schwalke; Introduction of Crystalline High-K Gate Dielectrics in a CMOS Process, SiO_2, Advanced Dielectrics and Related Devices, Chamonix Mont- Blanc, France, on June 21-23, 2004.

7. **R. Komaragiri**, U.Schwalke, Y.Stefanov, T.Ruland; Comparison of praseodymium oxide gate MOSFETs with conventional SiO_2 MOSFETs: A simulation study, pp. 462-464, International workshop on physics of semiconductor devices (IWPSD), Madras, India, 2003.

8. U.Schwalke, Y.Stefanov, **R. Komaragiri**, T.Ruland; Electrical Characterization of Crystalline Praseodymium Oxide High-k Gate Dielectric MOSFETs, pp. 247-250, Proceedings of 33rd European Solid State Device Research Conference (ESSDERC), 2003.

Journal papers

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Curriculum vitae

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